PCI Express® External Cabling Specification Revision 2.0

June 22, 2012

Revision	Revision History	DATE
1.0	Initial public release.	1/4/2007
2.0	Updated for new requirements, incorporated approved ECNs, and corrected typographical errors.	6/22/2012

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1. Introduction

This is a companion specification to the *PCI Express Base Specification*. Its primary focus is the implementation of cabled PCI Express®. The discussions are confined to copper cabling and their connector requirements to meet the PCI Express signaling needs at 5.0 GT/s. No assumptions are made regarding the implementation of PCI Express compliant Subsystems on either side of the cabled Link; e.g., PCI Express Card Electromechanical (CEM), ExpressCard™, ExpressModule™, PXI Express™, system board, or any other form factor. Such form factors are covered in other separate specifications.

1.1. Terms and Acronyms

Auxiliary signals	Signals not required by the PCI Express architecture, but necessary for certain desired functions or system implementation; for example, the CREFCLK signal.
Basic bandwidth	Contains one PCI Express Lane.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x4 to a collection of four PCI Express Lanes; etc.
Downstream	1. The relative position of an interconnect/system element (Port/component) that is farther from the Root Complex. Within the context of this specification also referred to as "Downstream Subsystem." 2. A direction of information flow where the information is flowing away from the Root Complex.
Endpoint	A device with a Type 00h Configuration Space header.
form factor	In the context of this specification, form factor refers to other specifications that could be used as the foundation for implementing an external cabled PCI Express Port; e.g., PCI Express Card Electromechanical, ExpressCard, ExpressModule, Compact PCI Express.
HCSL	High-speed Current Steering Logic implemented in various different clock generator components.
Host System	The compute entity which contains the PCI Express Root Complex and is the source of the reference clock signal. In the context of this specification, also referred to as "Upstream Subsystem."
Hot-Plug	Insertion and/or removal of a cable into an active Subsystem.
Lane	One PCI Express Lane contains a differential pair for Transmit and another differential pair for Receive. A by-N Link is composed of N Lanes.
Link	A collection of one or more PCI Express Lanes providing the communication path between an Upstream and Downstream Port.
Port	A group of Transmitters and Receivers located on the same device that define a Link when active.

Sideband signaling	A method for signaling events and conditions using physical signals separate from signals forming the Link between two components.
Subsystem	In the context of this specification, Subsystem is a generic term identifying either an Upstream or Downstream device providing a cabled PCI Express Port.
Wakeup	A mechanism used by a component to request the reapplication of main power when in the L2 Link state. Two such mechanisms are defined in the *PCI Express Base Specification*: Beacon and WAKE#.

1.2. Reference Documents

- *PCI Express Base Specification, Revision 2.0*
- *PCI Express Card Electromechanical Specification, Revision 2.0*
- *PCI Hot-Plug Specification, Rev. 1.1*
- *PCI Standard Hot-Plug Controller and Subsystem Specification, Rev. 1.0*
- *EIA 364 Series, Electrical Connector Test Procedures Including Environmental Classifications with Test Procedures*
- *EIA 364-1000, Environmental Test Methodology for Assessing the Performance of Connectors and Sockets used in Business Office Applications*

1.3. Documentation Conventions

Capitalization

Some terms are capitalized to distinguish their definition in the context of this document from their common English meaning. Words not capitalized have their common English meaning. When terms such as "memory write" or "memory read" appear completely in lower case, they include all transactions of that type.

Register names, and the names of fields and bits in registers and headers, are presented with the first letter capitalized and the remainder in lower case.

Signal Names

Within this specification, signal names are preceded with a "u", "C", or "d" character to identify the Upstream Subsystem, cable, or Downstream Subsystem respectively.

Numbers and Number Bases

Hexadecimal numbers are written with a lower case "h" suffix, e.g., FFFh and 80h. Hexadecimal numbers larger than four digits are represented with a space dividing each group of four digits, as in 1E FFFF FFFFh. Binary numbers are written with a lower case "b" suffix, e.g., 1001b and 10b. Binary numbers larger than four digits are written with a space dividing each group of four digits, as in 1000 0101 0010b.

All other numbers are decimal.

Implementation Notes

Implementation Notes should not be considered to be part of this specification. They are included for clarification and illustration only.

1.4. Specification Contents

This specification contains the following information:

- Subsystem requirements
- Sideband signaling and usage models
- Cable hot insertion and removal
- Subsystem electrical budgets
- Cable and connectors electrical budget
- Cable and connectors specifications
- Power provisioning

1.5. Objectives

The objectives of this specification are as follows:

- Define PCI Express external cables and associated connectors
- Support PCI Express data rates of up to 5.0 GT/s, while maintaining compatibility with the 2.5 GT/s signaling rate specifications
- Support standard PCI Express components, as defined by the *PCI Express Base Specification, Revision 2.0*
- Forward looking for future scalability
- Maximize cable interoperability for user flexibility
- Enable Hot-plug as a native function
- Allow revolutionary partitioning of the PC architecture
- Upgradeability
- Backwards compatibility with subsystems compatible with Revision 1.0 of this specification

1.6. Overview

PCI Express is the third generation of multi-purpose I/O interface that can be used across the computing industry, from mobile through high-end servers and communication equipment. The broad usage and versatility of this technology allows for system extensions to external input/output Subsystems that meet the needs for specific target applications and/or environments.

Cabled PCI Express targets a large number of applications, including but not limited to:

- Split-systems, or disaggregate PCs, with a desktop "console" that contains removable media drives (e.g., CD/DVD), memory modules, I/O ports (e.g., USB, IEEE-1394), and audio jacks
- I/O expansion to extend the I/O card capabilities of the main system for support of different form factors, including legacy, test and measurement, and instrumentation equipment
- Server expansion I/O to support conventional PCI Express add-in cards (with or without Hot-Plug support) and/or ExpressModules
- Location of the graphic subsystem (i.e., controller and memory) external to the main systems unit

System-level support for cabled PCI Express is possible through implementation on expansion cards; e.g., PCI Express CEM, ExpressModules, PXI Express, ExpressCard, or direct from a system board.

This specification defines connectors for supporting a x1, x4, x8, and x16 cabled copper PCI Express Links. Other Link widths, such as x2, might be added in subsequent revisions of this specification. Although some references are provided relating to optical interconnects, specific electrical and mechanical requirements for supporting such optical interconnects are beyond the scope of this specification.

Utilizing off-the-shelf PCI Express components is the focus of this specification, while providing enough flexibility for design and implementation of dedicated components for driving the cabled interconnect. As such, much of this specification builds upon other PCI Express form factor specifications.

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2. Auxiliary Signals

Auxiliary signals are provided on the connector to assist with system-level functionality or implementation. The high-speed differential signaling levels are compatible with advanced silicon processes while all low-speed Auxiliary signals are defined to be compatible with +3.3 V signaling.

Besides the signals that are required to transmit/receive data on the PCI Express interface, there are also signals that may be necessary to implement the PCI Express interface in a distributed system environment, or to provide certain desired functions, including power for data conditioning within the connector backshell. These signals are referred to as the auxiliary or sideband signals.

This specification describes the feature set from the cabled interface perspective. In other words, a required feature indicates that a wire interconnect shall be provided although this does not necessarily mean that the function needs to be implemented in a given Subsystem. Features that are optional for implementation by a Subsystem are explicitly defined as such in the following text.

The PCI Express cable connector and cabling support the following Auxiliary signals:

- CREFCLKp/CREFCLKn (required): Low voltage differential cable reference clock.
- CPRSNT# (required): Cable present detect, an active-low signal provided by a Downstream Subsystem to indicate that it's both present and its power is "good" (within tolerance).
- CPERST# (required): Cable PERST#, an active-low signal, logically equivalent to system PERST# (platform reset), driven by the Upstream Subsystem.
- CPWRON (required): Cable Power On, an active-high signal provided by an Upstream Subsystem to notify slave-type Downstream Subsystems to turn their main power on or off, used for example to put a slave Subsystem into the S3 power management state.
- SB_RTN (required): The SideBand Return provides a return current path for all single ended sideband signals, allowing for power domain isolation between Subsystems.
- CWAKE# (required): Cable Wake, an active-low signal that is driven by a Downstream Subsystem to re-activate the PCI Express hierarchy's main power rails and reference clocks. Although optional for Upstream and Downstream Subsystems, all cable assemblies shall include CWAKE#.
- +3.3 V POWER (optional for connector): Power provisioning to the connector backshell is provided to allow for active signal conditioning components within the cable assembly. A wire shall not be provided within the cable.
- PWR_RTN (optional for connector): Return path optional for +3.3 V power provisioning.

Power-domain isolation between Upstream and Downstream Subsystems is optional. Voltage differences between signal grounds at each end of the cable are implementation dependent. The SB_RTN signal is provided for applications that require power-domain isolation.

2.1. Signal Compatibility Matrix

All Auxiliary signals are required from a cabling perspective. While Subsystems may provide power to the cable connectors, there must be no current path via the cable for such power. In other words, a wire shall not be provided for power delivery via the cable. Some signals provide functionality that may not be required by all applications. Table 2-1 lists the signals that are optional for an Upstream and/or Downstream Subsystem, with a brief description on features enabled by it.

Table 2-1: Signal Compatibility Matrix

Signal	Signal Type	Upstream Subsystem	Cable Assembly	Downstream Subsystem	Comments
CREFCLK	Low Voltage Differential Current Mode (HCSL, LVPECL, etc.)	Required Output	Required	Optional Input	If not utilized at the Downstream Subsystem, it shall provide dual 50 Ω termination to ground. Implementation is required at the Upstream Subsystem for interoperability, providing a baseline feature set.
CPRSNT#	3.3 V Logic	Required Input	Required	Required Output	Required on both sides of the cable. The driver is open-drain type and requires high impedance during power off states.
CPERST#	3.3 V Logic	Required Output	Required	Optional Input	A Downstream Subsystem might choose to take advantage of inband reset communication only. The driver is open-drain type.
CPWRON	Pull-up Resistor or 3.3 V Logic	Required Output	Required	Optional Input	Supports features such as dynamic power sequencing and power management states. Implementation is required at the Upstream Subsystem for interoperability, providing a baseline feature set.
CWAKE#	3.3 V Logic	Optional Input/Output	Required	Optional Output/Input	Optional on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. This signal becomes bidirectional if both ends support OBFF.

Signal	Signal Type	Upstream Subsystem	Cable Assembly	Downstream Subsystem	Comments
SB_RTN		Required	Required	Required	Required on both sides of the cable. Downstream Subsystems implementing power domain isolation shall not connect this directly to ground potential, instead use it as a current return path and potentially as a reference.
POWER / PWR_RTN		Optional	NW (No Wire)	Optional	Power provisioning is optional from both sides of the cable. At no time, shall wires be implemented within the cable assembly.

2.2. Power-Domain Isolation

Requirements for power-domain isolation are application specific and closely tied with the geographic utilization of the equipment as well as cable length. Two similar sideband signaling implementations are provided.

The power-domain isolation case is depicted in the various figures contained within this chapter using opto-isolator technology. Implementation of opto-isolators is not a requirement although similar or improved performance and functionality shall be obtained with alternate technology choices for implementing power-domain isolation.

Implementation of non-isolated cabled applications is very similar to the power domain isolation case and, for this reason, is not described in as much detail. Any figure, within this chapter, containing an opto-isolator would replace such with an open-drain logic component. An opto-isolator is in essence an open-drain component with the additional isolation feature.

From the Upstream Subsystem perspective, there is no difference in implementation for supporting either model. It is the Downstream Subsystem designer's responsibility to evaluate any isolation requirements for each particular application.

2.3. Cable Reference Clock (Required)

To control jitter, radiated emissions, and crosstalk, and allow for future silicon fabrication process changes, a low voltage swing, differential clock is specified.

Isolated power domains, between the two Subsystems, are maintained through implementation of AC-coupling capacitors at the source. Both source and load termination are required for reducing signal reflections and improving signal integrity.

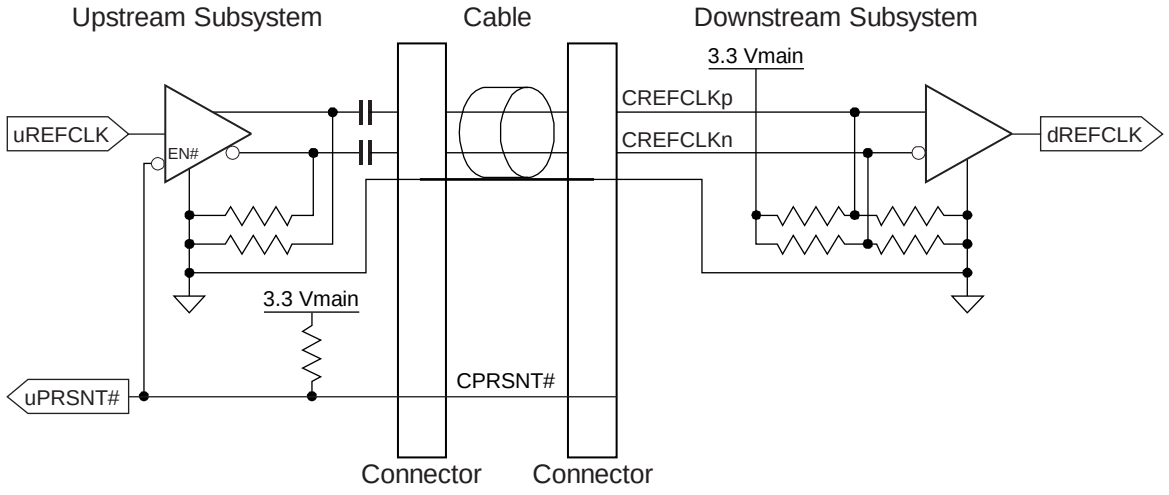


Figure 2-1: CREFCLK Implementation Description

Supplying the cable reference clock is required from an Upstream Subsystem. Although recommended, utilizing this clock is optional for the Downstream Subsystem. In cases where a Downstream Subsystem does not take advantage of this clock it shall provide proper termination, implemented as two 50 Ω (±1%) resistors to ground. Clocking dependencies described in Sections 2.3.1 and 2.3.2 hold true with all implementation choices.

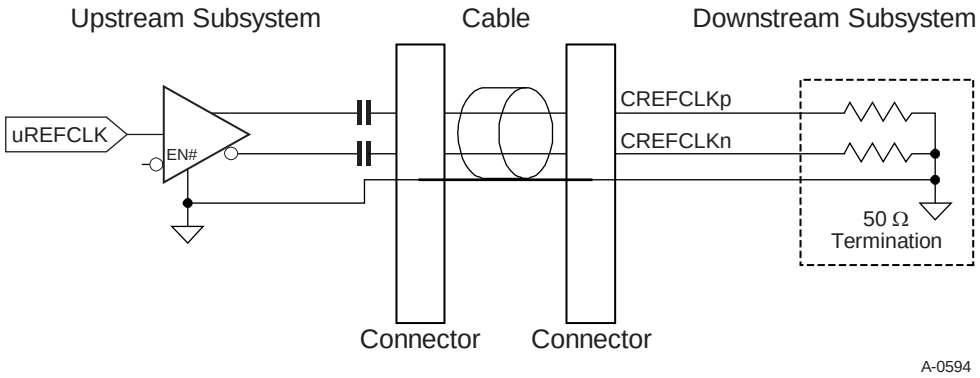


Figure 2-2: Terminating Unused CREFCLK

The Cable Reference Clock (CREFCLKp/CREFCLKn) shall be disabled at the source unless both sides of the Link are powered and the cable is installed, preventing any glitches and excessive EMI that could result from unterminated signals. With the clock being an AC-coupled differential signal, tri-state logic or forcing the clock inactive through other means are allowed. Gating of the cable reference clock, as shown in Figure 2-1 using the Cable Present Detect (CPRSNT#) signal, is required by this specification to prevent reliability problems. Components might be sensitive to, and damage can result from, providing a clock signal while power rails are not at their normal operating levels.

This specification makes no assumptions on the clock signaling provided from a system clock generator to a potential cable driver. It is the responsibility of the designer to provide any necessary signal translation based on the target implementation; i.e., system board, PCI Express add-in cards, or any future form factors supported with PCI Express signaling. Only the Cable Reference Clock requirements are specified herein.

CREFCLK shall be implemented using good design practices for high-speed differential signaling. A differential trace impedance of 100 Ω ±10% is recommended.

2.3.1. Clocking Dependencies

Accuracy, in parts per million (ppm), of the 100 MHz reference clock shall meet the requirements set by Chapter 4 of the *PCI Express Base Specification* across a range of phase delays expected over a cable.

2.3.2. Spread Spectrum Clock (SSC) Sources

Spread Spectrum modulation is supported and, if utilized, shall meet the requirements set by Chapter 4 of the *PCI Express Base Specification*. Also, the same considerations and limitations apply to cabled PCI Express usage models.

2.3.3. AC-coupling

The Cable Reference Clock shall be AC-coupled at the Upstream Subsystem (the source) transmitting the differential clock. A recommended value is 0.1 µF although other capacitor values are allowed within the signal integrity and rise/fall time specifications provided within Section 2.12.3.

2.3.4. Impact of Jitter on Bit Error Ratio (BER)

An increase in Bit Error Ratio (BER) can result from phase jitter content on the cable reference clock. Increases in eye closure can also result from the round-trip signal delay of the cabled Link, rise/fall time degradation of the reference clock, and implementation specific Clock Data Recovery circuits of PCI Express components, in addition to the losses induced by the Link. Thorough system level phase jitter consideration and simulation are recommended. Refer to whitepapers available from the PCI-SIG and Section 2.12.4 for more information.

It should be realized that system level phase jitter considerations do exist even when operating with independent clocks, without SSC, at both ends of a Link.

2.3.5. CREFCLK Distribution

Jitter budgeting within this specification assumes both sides of the cabled Link operate off of common 100 MHz reference clocks, distributed via the cable, with identical phase jitter magnitude over the spectrum of concern. Applications requiring dedicated buffers for driving the cable reference clock should maintain this phase jitter magnitude and spectrum requirement. Improper termination, intra-pair skew, and crosstalk can have a significant impact on phase jitter and potentially render a Link inoperable.

A timing relation between CREFCLK and the reference clock driving the Upstream cabled PCI Express Receiver (uREFCLK) is specified below; see Figure 2-3. This clock skew is measured at the Upstream Board-Side connector, measurement point T1, with respect to point T2 at the pads of the transceiver. Bit Error Ratio (BER) calculations within this specification are based on the following timing requirement: T1 = T2 ± 1 ns ($t_{CLK-SKEW}$ as specified in Table 2-3).

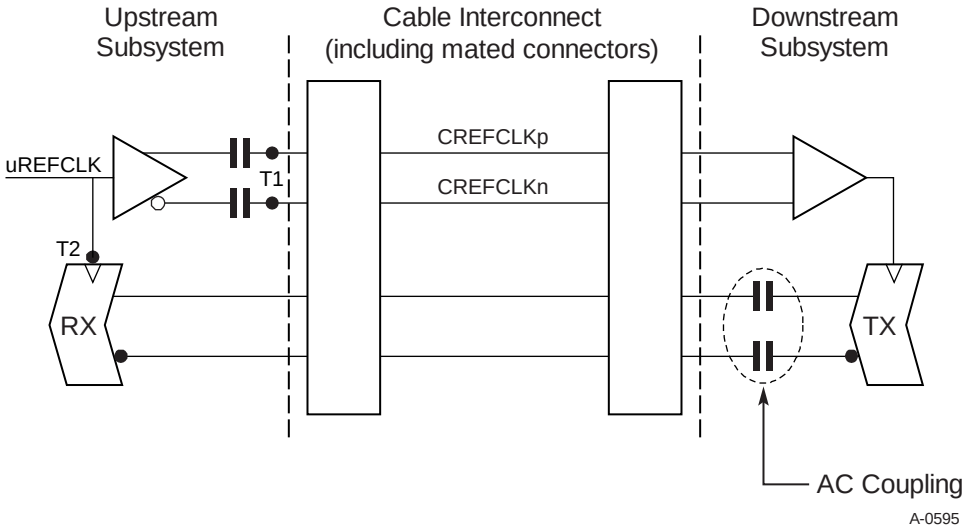


Figure 2-3: CREFCLK Timing Skew

2.4. Cable Present (Required)

A Downstream Subsystem present detection mechanism is specified, through CPRSNT#, to provide the following functionality:

- Hot-Plug support
- Power Good signaling (to Upstream Subsystem)
- Cable reference clock output control
- End-user diagnostics for cable presence

PCI Express Hot-Plug, with legacy operating systems, can be supported by connecting CPRSNT# within the Upstream Subsystem to the presence detect input of a Downstream Port of an Upstream Subsystem (e.g., a Root Complex Port or the Downstream Port of a PCI Express Switch), or by using Hot-Plug Surprise mechanisms. See the *PCI Express Base Specification, Revision 2.0* or later for information about PCI Express Hot-Plug.

Following a Hot-Plug event, a delay circuit within the Upstream Subsystem guarantees a minimum CPERST# pulse as defined within Section 2.5.

Power Good signaling is accomplished with the following signals: CPERST#/CPWRON, for signaling the status of the Upstream Subsystem, and CPRSNT# as described within this section. CPRSNT# assertion by the Downstream Subsystem is qualified by the power good condition of the Downstream Subsystem, as illustrated in Figure 2-4. This provides a mechanism for the Upstream Subsystem to determine whether the power is good within the Downstream Subsystem, enable the reference clock, and initiate Link Training.

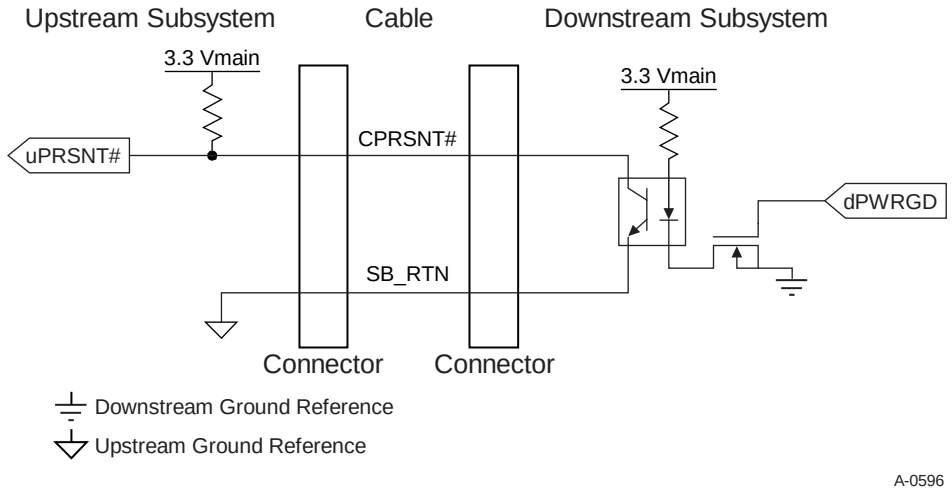


Figure 2-4: CPRSNT# Signaling with Power Isolation

PCI Express components within Downstream Subsystems could potentially be damaged if they receive a cable reference clock while their power provisioning is not at normal operating levels. Gating of the cable reference clock, using the Cable Present Detect (CPRSNT#) signal, is required by this specification to prevent reliability problems. This is illustrated in Figure 2-1.

As part of determining why a computer system is not working correctly, CPRSNT# provides information that can be used to help end users diagnose whether the cable is connected properly. How this might be accomplished is beyond the scope of this specification.

Implementations of CPRSNT# shall be designed such that:

- Unpowered CPRSNT# output circuits are not damaged if a voltage is applied to them from other powered sources.
- When power is removed from the CPRSNT# generation logic, the unpowered output does *not* present a low-impedance path to ground or any other voltage.

These additional requirements ensure that the CPRSNT# signal continues to function properly. It is important to note that most commonly available open-drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CPRSNT#.

2.5. Cable Platform Reset (Required)

Cable Platform Reset (CPERST#) is driven by the Upstream Subsystem to provide the Downstream Subsystem an indication of the power state and reset state of the Upstream Subsystem. CPERST# is required to remain asserted while CPRSNT# is de-asserted. Figure 2-10 illustrates a related timing requirement.

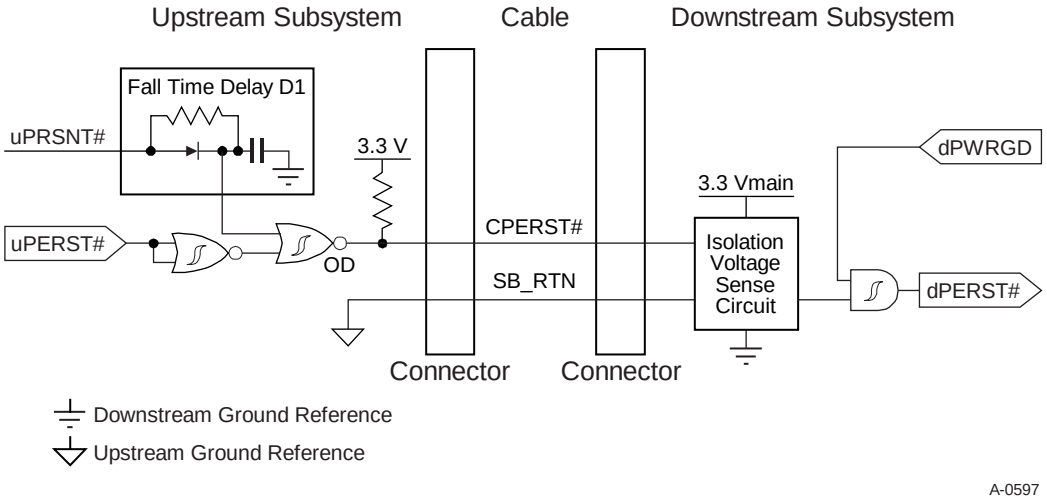


Figure 2-5: CPERST# Signaling with Power Isolation

Parameter $t_{CLK\text{-}PERST}$ specifies the CREFCLK stability period relative to CPERST# assertion at the Upstream cable connector. Refer to Figure 2-6 and Table 2-3 for Upstream system timing requirement.

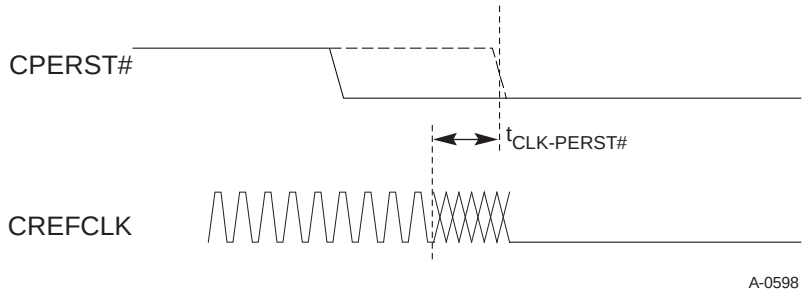


Figure 2-6: CPERST# to CREFCLK Timing

A potential issue arises if the CPERST# delay through a cable driver and/or Receiver circuit is longer than the total buffering delay for CREFCLK (if any). During power down or S0 to S3/S4 sequences, dPERST# within the Downstream Subsystem may be asserted after dREFCLK becomes

no-longer stable, which may cause undefined behavior by components within the Downstream Subsystem.

It is the responsibility of the Downstream Subsystem to correct for cable induced skew between CREFCLK and CPERST#, and provide an appropriate logic implementation, or guarantee it is immune to CREFCLK going invalid shortly before CPERST# is asserted. Inserting additional delay into the reference clock is not recommended due to the impact on system level phase jitter and resulting eye closure.

Fall delay D1 is used to meet timing requirement $T_{PERST\#-PRSNT\#}$ as illustrated in Figure 2-10. This provides a minimum CPERST# pulse following a Hot-Plug event. Refer to Section 2.11 and Table 2-3 for details.

2.6. Cable Power On (Required)

CPWRON shall be implemented within the cable assembly and shall be provided by the Upstream Subsystem to, for example, allow for control of the main power within Downstream Subsystems. Implementation within Downstream Subsystems is optional.

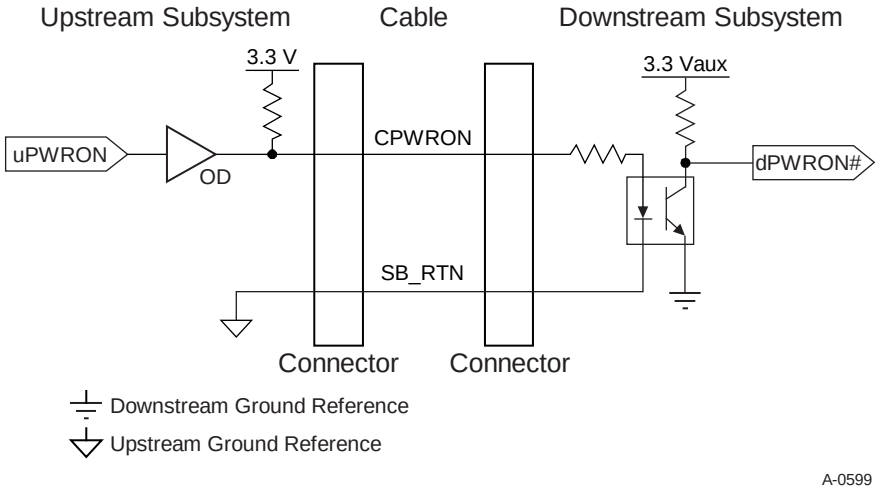


Figure 2-7: CPWRON Signaling with Power Isolation

A timing requirement (t_{CPWRON}) from Upstream power-on (voltage rails within the Upstream Subsystem reaching nominal value) to CPWRON being asserted at the Upstream connector is illustrated in Figure 2-8 and Table 2-3. This timing specification forms a basis to allow designers of Downstream Subsystems to meet their specific implementation requirements.

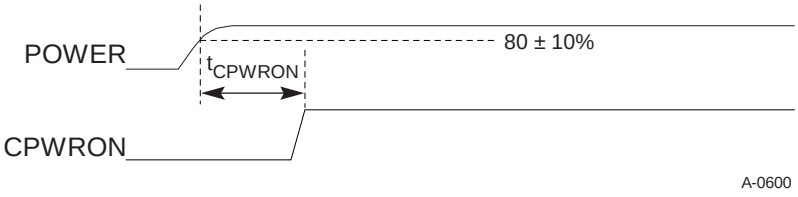


Figure 2-8: CPWRON Timing

Some key considerations as to whether a given application can benefit from using CPWRON are provided with the following usage scenarios:

- If the overall system is in the S3 state; i.e., components are about to transition from $D3_{hot}$ to $D3_{cold}$, CPWRON may be needed to turn the Downstream Subsystem's main power off.
- If the overall system is in the S3 state; i.e., components in $D3_{cold}$, and a wake event is generated, the CPWRON signal may be needed to turn the Downstream Subsystem's power on.
- Downstream Subsystems utilizing CPWRON for automatic power sequencing should consider ramp-up times required of their main supplies. Upstream systems specify a minimum delay from power valid to uPERST# de-assertion. Any Downstream Subsystem supporting this power sequencing feature should guarantee it is able to engage in PCI Express Receiver detection, and subsequent Link Training Sequence, before being initiated from the Upstream Port.

A cable driver/buffer implemented at the Upstream Subsystem shall be an open-drain type or similar technology. The purpose is to prevent component damage in such case where, in error, two Upstream systems are cabled together. As the intent is to provide early power status notification from the Upstream Subsystem, no specific rise/fall time requirements are imposed.

2.7. Sideband Return (Required)

SB_RTN provides a return current path for all single-ended sideband signals, to allow for power domain isolation between Subsystems. SB_RTN shall be connected to signal ground within the Upstream Subsystem and, when supporting power domain isolation, shall not be connected to ground potential of the Downstream Subsystem.

With a power domain isolation usage model, SB_RTN can also be used as a reference voltage for Downstream Subsystems to accurately sense the voltage on CPERST# and CPWRON, compensating for any DC voltage difference between signal grounds at each end of the cable.

Downstream Subsystems that do not incorporate power domain isolation shall provide a direct connection of SB_RTN to a logic-ground potential. Specifications for worst-case signal output and input levels are inclusive of any DC-voltage difference between the signal grounds at each end of the cable. This places a limit on the maximum DC resistance of the cable assembly and, therefore, limits the maximum supported cable length. Refer to Section 6.2.2 for cable electrical performance requirements.

2.8. Cable WAKE# (Required)

CWAKE# is an active-low signal asserted by a Downstream Subsystem to reactivate the system hierarchy's main power rails and reference clocks. Support of CWAKE# functionality is optional for both the Upstream and Downstream Subsystems; however, all cable assemblies shall include CWAKE# connectivity. Only Subsystems that support the wake process connect to this pin. If a Subsystem has wakeup capabilities, it shall support the CWAKE# function. Such Subsystems are not required to support Beacon as a wakeup mechanism, but are strongly encouraged to support it. The assertion and de-assertion of CWAKE# are asynchronous to any system clock. See Chapter 5 of the *PCI Express Base Specification* for more details on PCI-compatible power management.

If the CWAKE# signal is supported by a Subsystem, implementation guidelines governed by the target form factor specification(s) shall be followed. One possible CWAKE# implementation is illustrated in Figure 2-9.

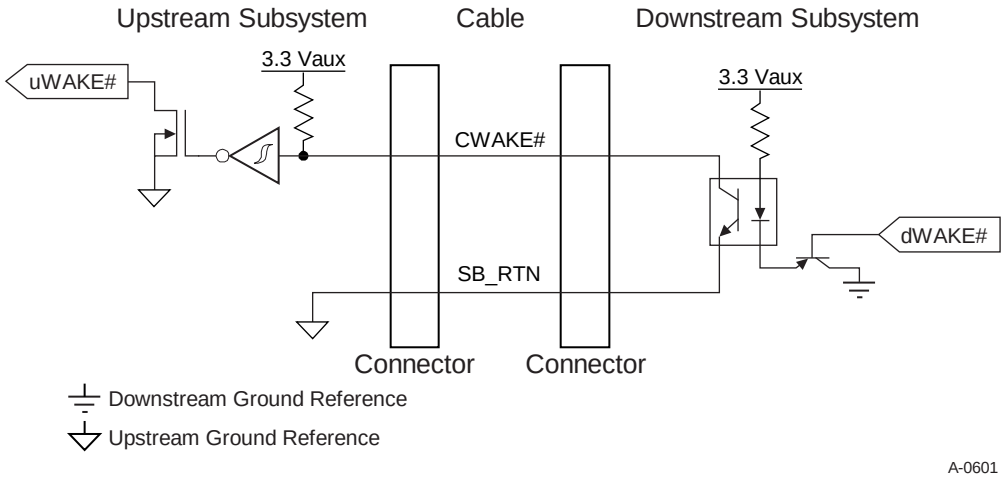


Figure 2-9: CWAKE# Signaling with Power Isolation

CWAKE# shall not be bussed between multiple connectors for external cabling. Hot-Plug requires that CWAKE# be isolated between connectors and de-asserted during Hot-Plug/Hot Removal events.

CWAKE# has additional electrical requirements over and above standard open-drain signaling. For example, these requirements allow it to be shared between devices that are powered off and those that are powered on using auxiliary power. The additional requirements include careful circuit design to ensure that a voltage applied to the CWAKE# signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, in all cases, the device shall ensure that it does not pull CWAKE# low unless CWAKE# is being intentionally asserted, including when the related function is in $D3_{cold}$.

This means that any component implementing CWAKE# shall be designed such that:

- Unpowered CWAKE# output circuits are not damaged if a voltage is applied to them from other powered sources of CWAKE#.
- When power is removed from its CWAKE# generation logic, the unpowered output does *not* present a low-impedance path to ground or any other voltage.

These additional requirements ensure that the CWAKE# signal network continues to function properly. It is important to note that most commonly available open-drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CWAKE#.

Subsystems are permitted to generate the Beacon wakeup mechanism in addition to using the CWAKE# mechanism, although the Upstream Subsystem is not required to provide support for Beacon.

Note: If the Downstream Subsystem uses the Beacon mechanism in addition to the CWAKE# sideband signal, the Beacon may be ignored by the Upstream Subsystem. Circuits that support the

wake function and are intended to work in any PCI Express environment should be designed to generate the Beacon on their PCI Express data lines.

Subsystem designers must be aware of the special requirements that constrain CWAKE# and ensure that their implementation does not interfere with the proper operation of the CWAKE# network. The CWAKE# input into the Upstream Subsystem, with copper cabling, may de-assert as late as t_{CWKRF} after the CWAKE# output from the Downstream Subsystem de-asserts; i.e., the CWAKE# pin shall be considered indeterminate for some period after it has been de-asserted.

OBSERVATION: The Optimized Buffer Flush/Fill, or OBFF, mechanism that utilizes the CWAKE# signal may not be compatible with some designs. Opto-isolation or other electrical isolation circuit implementations may prevent bidirectional signaling. To utilize the OBFF functionality, it is recommended to use the message-based mechanism over the cable.

2.9. Power (Optional +3.3 V)

Power provisioning to the cable connector backshell allows active circuitry to be designed as part of the cable assembly. However, details of such active circuit design are often proprietary in nature and beyond the scope of this specification. There are also risk factors, associated with long cables, that need to be overcome. Refer to Section 4.2 for additional information on some of these risks. Note that wires shall *not* be implemented in the cable for delivery of power between Subsystems.

Potential applications are as follows:

- Active equalization for extended copper cable lengths
- E-O (Electrical-Optical) transceivers for optical interconnects

Voltage provided is +3.3 V (±9%) as this is the lowest common power rail available. Current levels vary between different supported Link widths; refer to Table 2-2. Implementation of current limiting features, and other potential safety requirements, is strongly recommended.

2.10. ESD

Electrostatic Discharge (ESD) requirements for auxiliary signals are identical to the specified PCI Express signal protection. Refer to Section 3.4 for ESD requirement details.

2.11. Power Sequencing

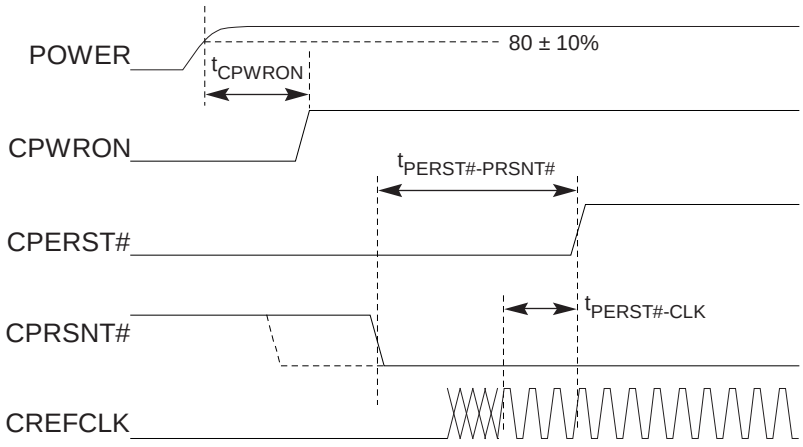
2.11.1. Power-Up Sequencing

Figure 2-10 illustrates power-up sequencing resulting from a cold-boot or Hot-Plug event. From the Upstream Subsystem perspective, the following occur:

1. Power to the connector backshell is applied and CPWRON asserted.
2. CPRSNT# is asserted from the Downstream Subsystem.
   a. If the Downstream Subsystem is not powered on, this signaling will be postponed until the Subsystem is activated.
   b. CPRSNT# enables the Upstream CREFCLK driver.
3. CPERST# is de-asserted.
   a. CREFCLK has a timing relationship of $t_{CLK\text{-}PERST\#}$ with respect to CPERST# de-assertion.

The Downstream Subsystem responds as follows:

1. Based on the assertion of CPWRON, it may initiate power-up sequencing.
2. CPRSNT# is asserted.
3. The assertion of CPRSNT# enables CREFCLK.



Notes:

1. $t_{PERST\#-PRSNT\#}$ is the minimum time CPRSNT# asserted to CPERST# de-asserted.
2. $t_{PERST\#-CLK}$ is the minimum time CREFCLK stable to CPERST# de-asserted.
3. t_{CPWRON} is the maximum time from upstream power supply(s) reaching the 80% level to CPWRON asserted.

A-0602

Figure 2-10: Power-up Sequencing

2.11.2. Power-Down Sequencing

Figure 2-11 illustrates power-down sequencing resulting from a graceful or Hot-Unplug event. From the Upstream Subsystem perspective, the following occur:

1. CPERST# is asserted before power is outside of regulation limits.
   a. One exception is a Hot-Unplug event.
2. CREFCLK is guaranteed valid until $t_{CLK-PERST\#}$ before CPERST# is asserted.
3. As a result of power going outside of regulation, CPWRON goes inactive.
   a. During a Hot-Unplug event, the timing relationship between CPERST# and CPWRON cannot be guaranteed. Both signals are disconnected and it is the responsibility of the Downstream Subsystem to enter a reset state and/or enter a low-power state if supported. It cannot be assumed that CPERST# and CPWRON disconnect in any particular order.

The Downstream Subsystem responds as follows:

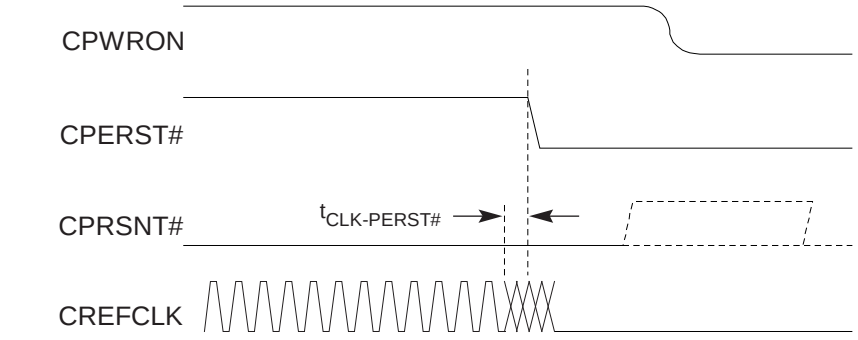
1. Based on the de-assertion of CPWRON, it may initiate power-down sequencing.

2. As a result of power going outside of regulation limits, CPRSNT# is de-asserted.

   a. In the event of a graceful shutdown, the Upstream Subsystem's power rails are outside of regulation limits thus the de-assertion of CPRSNT# is ignored.

3. The de-assertion of CPRSNT# disables CREFCLK (if still active).

   a. A race condition exists where CREFCLK tri-state/disable is initiated by either the Upstream Subsystem's power down or CPRSNT# de-assertion. Both accomplish the appropriate behavior.



Note:

1. $t_{CLK-PERST\#}$ is the minimum time from CPERST# active to CREFCLK no longer stable.

A-0603

Figure 2-11: Power-Down Sequencing

In the case where a Downstream Subsystem is shutdown independently from the Upstream Subsystem, CPRSNT# will assert. Following this assertion of CPRSNT# the Upstream Subsystem will disable the CREFCLK signal and assert CPERST#. This required behavior is described by the text in this chapter and is not depicted in Figure 2-11.

2.11.3. Power Management Sequencing

Figure 2-12 illustrates S0 to S3/S4 timing and also S3/S4 to S0 sequencing. Support of such power management states is optional; although, when implemented shall adhere to the requirements provided within this specification.

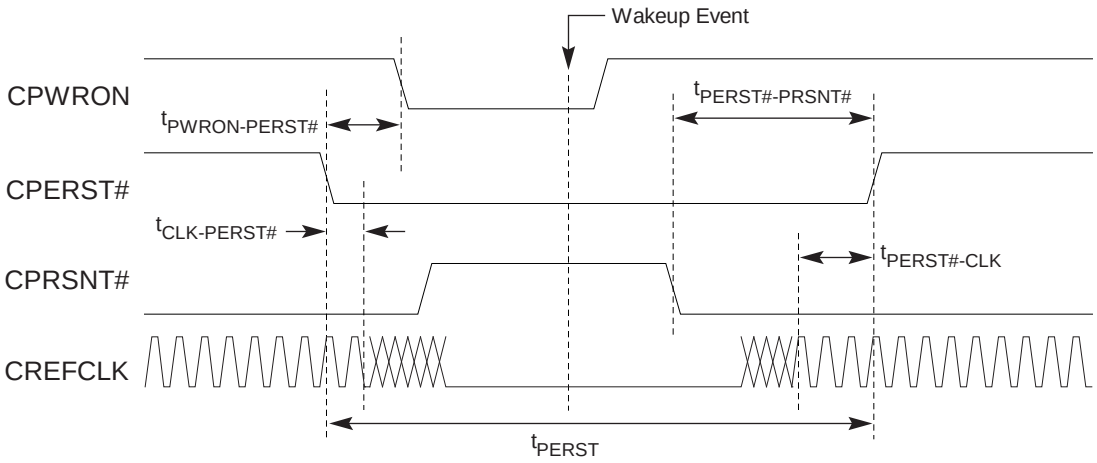
From the Upstream Subsystem perspective, the following occur when entering low-power states:

1. CPERST# is asserted before power is outside of regulation limits.
2. CREFCLK is guaranteed valid until $t_{CLK\text{-}PERST\#}$ before CPERST# is asserted.
3. As a result of power going outside of regulation, CPWRON goes inactive.

The Downstream Subsystem may respond as follows:

1. Following the de-assertion of CPWRON, it may initiate power-down sequencing.
2. As a result of power going outside of regulation limits, CPRSNT# is de-asserted.
3. The de-assertion of CPRSNT# disables CREFCLK (if still active).

A wakeup event generated from either the Upstream or Downstream Subsystem initiates a power-up sequence with identical timing as that described in Section 2.11.1.



Notes:

1. A wakeup event resumes power to the connector (if provided), restarts the clock, and the sequence proceeds as in power up.
2. The minimum active time for CPERST# is t_{PERST}.
3. $t_{PWRON-PERST\#}$ is the minimum from CPERST# asserted to CPWRON inactive.
4. $t_{PERST\#-CLK}$ is as defined for power-up sequencing.
5. $t_{PERST\#-PRSNT\#}$ is as defined for power-up sequencing.
6. $t_{CLK-PERST\#}$ is as defined for power-down sequencing.

A-0604

Figure 2-12: Power Management Sequencing (S0 to S3/S4 to S0)

2.12. Auxiliary Signal Parametric Specifications

2.12.1. DC Specifications for Single-Ended Signals

Table 2-2: DC Specifications

Symbol	Parameter	Signal	Conditions	Min	Max	Units	Notes
V_{OL}	Output Low Voltage	CPERST#	I_{OL} = 0 mA		0.4	V	1, 3
		CPRSNT#, CWAKE#	I_{OL} = 8 mA				2, 3
V_{OH}	Output High Voltage	CPERST#, CPWRON	I_{OH} = 0 mA	3.0	3.6	V	1
		CPRSNT#, CWAKE#					2
I_{OH}	Output High Current	CPWRON, CPERST#	V_{OH} =0 V		12	mA	1, 5, 6
			V_{OH} = 1.0 V	6.0	11		1, 5
			V_{OH} = 2.4 V	2.5			1, 5
I_{OL}	Output Low Current	CPWRON, CPERST#			18	mA	1, 5, 7

Symbol	Parameter	Signal	Conditions	Min	Max	Units	Notes
I_{LEAK}	Output Leakage Current	CPRSNT#, WAKE#	V_O = 3.3 V		10	µA	2, 3, 9
V_{IL}	Input Low Voltage	CPWRON, CPERST#			0.8	V	2, 10, 11
		CPRSNT#, CWAKE#					1, 4, 11
V_{IH}	Input High Voltage	CPWRON, CPERST#	I_{IH} <= 2.5 mA	2.0		V	2, 10
		CPRSNT#, CWAKE#	I_{IH} = 0 mA				1, 4
V_{IPU}	Input Pull Up Voltage	CPRSNT#, WAKE#	I_{OH} = 0 mA	3.0	3.6	V	1, 4
V_{PWR}	Power Pin Voltage	POWER	x1: 0 - 0.35 A x4: 0 - 0.75 A x8: 0 - 1.5 A x16: 0 - 2.5 A	3.0	3.6	V	1, 3, 8

Notes:

1. Measured at the Upstream Subsystem connector and referenced to the SB_RTN pin.
2. Measured at the Downstream Subsystem connector and referenced to the SB_RTN pin.
3. Open-Drain output.
4. The input to the Upstream Subsystem includes a 1 kΩ (±5%) pull-up resistor connected to a +3.3 V power rail. The CWAKE# pull-up resistor shall be connected to a +3.3 Vaux rail if supported by the Upstream Subsystem.
5. The suggested Upstream implementation is an open-drain output driver and a 330 Ω (±5%) pull-up resistor connected to a +3.3 V power rail. The open-drain driver is optional for CPWRON. If an open-drain output driver is implemented, it shall meet these requirements.
6. The Upstream device shall limit its high-state output current to this value when its output is shorted to ground.
7. The Upstream device shall be capable of continuously sinking this much current from the cable when in the low state. This is to prevent damage when two Upstream devices are erroneously connected together.
8. Specified total current is distributed across the full set of POWER pins for any given connector.
9. I_{LEAK} specifies the maximum leakage current of the Downstream Subsystem when the signal is either deasserted or this Downstream Subsystem is powered down. This applies to both CPRSNT# and CWAKE#.
10. The Downstream CPWRON and CPERST# shall be implemented such that they sense logical low states when not connected to an Upstream device.
11. Implementations sensitive to voltage drop across the cable, such as the non-isolated architecture, shall consider a maximum cable DC resistance of 10 Ω.

2.12.2. AC Specifications for Single-Ended Signals

Table 2-3: AC Specifications For Single-Ended Sideband Signals

Symbol	Parameter	Min	Max	Units	Notes	Figure
$t_{PERST\#-PRSNT\#}$	CPRSNT# Asserted to CPERST# De-asserted	5	50	ms	3	2-10
$t_{PERST\#-CLK}$	CREFCLK Stable to CPERST# De-asserted	100		µs	1, 2, 3	2-10
$t_{CLK-PERST\#}$	CPERST# Asserted to CREFCLK No Longer Stable	-20		ns	1, 2, 3	2-11
$t_{PWRON-PERST\#}$	CPERST# Asserted to CPWRON De-asserted for S0 to S3/S4 Power Management Transition	0		µs		2-12
t_{PERST}	Minimum CPERST# Active Time	100		µs		2-12
t_{CWKRF}	CWAKE# Rise/Fall Time		200	µs		
t_{CPWRON}	Power Valid to CPWRON Valid		100	µs	3	2-7

Notes:

1. CREFCLK active means that CREFCLKp/n are being driven. CREFCLK is stable when it meets all the requirements specified for CREFCLK.
2. CPERST# is asynchronous to CREFCLK.
3. As measured at the Upstream Subsystem cabled connector interface.

2.12.3. Cable Reference Clock Specification

Table 2-4 provides the signaling requirements at the connector for the clock source in the Upstream Subsystem and the worst-case differential signaling the associated Receiver at the Downstream Subsystem should expect.

Table 2-4: Reference Clock Source AC Timing

Symbol	Parameter	100 MHz		Unit	Notes
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	6.0	V/ns	2, 3, 9
Fall Edge Rate	Falling Edge Rate	0.6	6.0	V/ns	2, 3, 9
V_{OH}	Differential Output High Voltage	+400		mV	2, 9
V_{OL}	Differential Output Low Voltage		-400	mV	2, 9
V_{IH}	Differential Input High Voltage	+200		mV	2
V_{IL}	Differential Input Low Voltage		-200	mV	2
V_{DIFF_MAX}	Maximum Differential Amplitude		2100	mV	2, 9
V_{CROSS}	Minimum and Maximum V_{CROSS}	-70	+70	mV	4, 9
V_{CROSS_DELTA}	Variation of V_{CROSS} Over All Rising Clock Edges		140	mV	1, 4, 8, 9
$t_{CLK-SKEW}$	uREFCLK to CREFCLK Skew at upstream subsystem	-1.0	+1.0	ns	3, 4, 14, 15, 17
V_{RB}	Ring-back Voltage Margin	-350	+350	mV	2, 9, 10
T_{STABLE}	Time Before V_{RB} is Allowed	500		ps	2, 9, 10
T_{PERIOD_AVG}	Average Clock Period Accuracy	-300	+2800	ppm	2, 11
T_{PERIOD_ABS}	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 5
$T_{CCJITTER}$	Cycle-to-Cycle Jitter		150	ps	2, 9
$T_{PHASEJITTER}$	Phase Jitter		86	ps	2, 9
$T_{PHASEJITTER\_5G}$	Phase Jitter for 5.0 GT/s		3.1	ps, RMS	2, 9, 13, 16
V_{SWING_MAX}	Absolute Max Output Swing		1050	mV	1, 6, 9
V_{SWING_MIN}	Absolute Min Output Swing		400	mV	1, 7, 9
V_{SYM}	Symmetry of Signal Swing and Level		10	%	1, 9
Duty Cycle	Duty Cycle	40	60	%	2, 9
Rise-Fall Matching	Rising Edge Rate (REFCLKp) to Falling Edge Rate (REFCLKn) Matching		20	%	1, 9, 12

Symbol	Parameter	100 MHz		Unit	Notes
		Min	Max		
Z_{C_SRC}	Clock upstream source impedance	40	60	Ω	1
Z_{C_LOAD}	Clock downstream load impedance	40	60	Ω	1

Notes:

1. Measurement taken from single-ended waveforms.
2. Measurement taken from differential waveforms. Either single-ended probes with math or a differential probe can be used for differential measurements.
3. Measured from -150 mV t0 +150 mV on the differential waveform (derived from CREFCLKp minus CREFCLKn). The signal shall be monotonic through the measurement region for rise and fall time. The 300 mV measurement window, of the clock source and Receiver respectively, is centered on the differential zero crossing.
4. Measured at the crossing point where the instantaneous voltage value of the rising edge of CREFCLKp equals the falling edge of CREFCLKn. See Figure 2-13.
5. Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation. See Figure 2-16.
6. Defined as the maximum single-ended voltage swing. See Figure 2-13.
7. Defined as the minimum single-ended voltage swing. See Figure 2-13.
8. Defined as the total variation of all crossing voltages of rising CREFCLKp and falling CREFCLKn. This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 2-13 and Figure 2-14.
9. Upstream Subsystem compliance is measured at the connector using the circuit of Figure 2-19 and Downstream Subsystem compliance of CREFCLKp and CREFCLKn are measured at the load capacitors C_L. Test load C_L = 2 pF, R_{TD} = 50 Ω. Phase jitter requirements are provided in Section 2.12.4.
10. T_{STABLE} is the time the differential clock shall maintain a minimum Vol/Voh differential output voltage after rising/falling edges before it is allowed to droop. T_{STABLE} and V_{RB} are measured at the Upstream Subsystem connector interface. See Figure 2-18.
11. PPM refers to parts per million and is a period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM, then, we have an error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum. For systems employing Spread Spectrum, there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800 PPM.
12. Matching applies to rising edge rate for CREFCLKp and falling edge rate for CREFCLKn. It is measured using a ±75 mV window centered on the median cross point where CREFCLKp rising meets CREFCLKn falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CREFCLKp should be compared to the Fall Edge Rate of CREFCLKn. The maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 2-15.
13. Analysis requirements for phase jitter requirements for 5.0 GT/s are provided in Section 2.12.4.
14. Refer to Figure 2-3.
15. As measured at the upstream subsystem cabled connector interface.
16. There is a relationship between the amount of jitter calculated and the edge rate of the captured waveform when data is captured with an oscilloscope. A waveform with a slow edge rate will report a higher jitter value due to sampling phenomena and interpolation. It is recommended that the clock waveform be captured with the least amount of disturbance to the edge rate in order to get a more accurate analysis of the jitter output from the clocking system. To minimize edge distortions, the edge should be transmitted with

no reduction in bandwidth and the resolution should be high enough to accurately capture the edge of the signal without using interpolation.

17. A clock skew requirement, REFCLK driving the Upstream Receiver and CREFCLK at the Upstream cable connector, is imposed to bound the overall round-trip delay and its impact on eye closure. This timing requirement is with respect to the rising edge of the differential waveform.

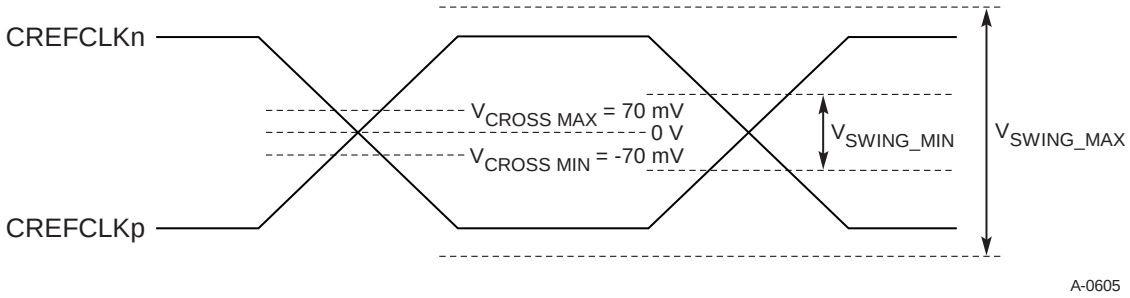


Figure 2-13: Single-Ended CREFCLK Waveform

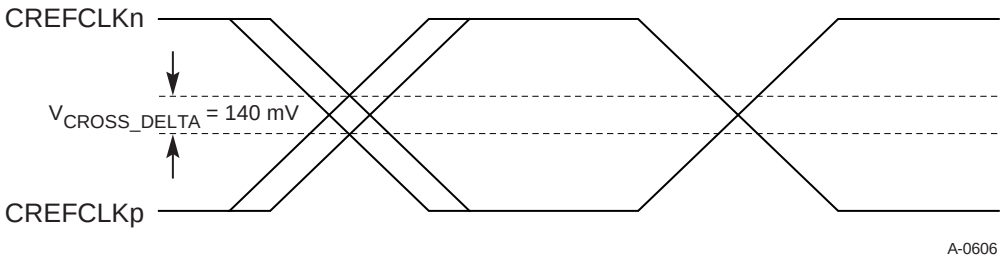


Figure 2-14: Single-Ended Measurement Points for Delta Cross Point

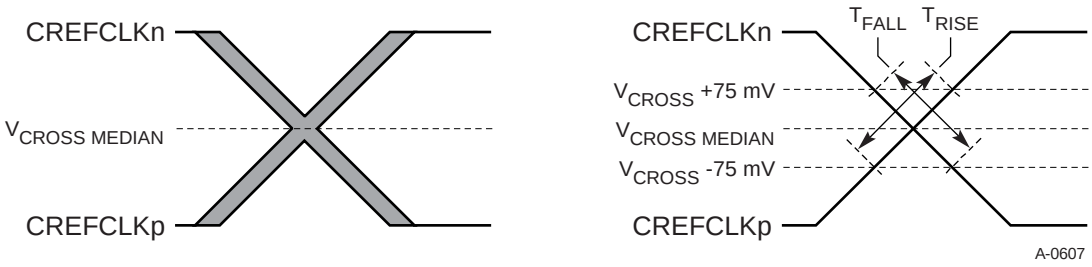


Figure 2-15: Single-Ended Measurement Points for Rise and Fall Time Matching

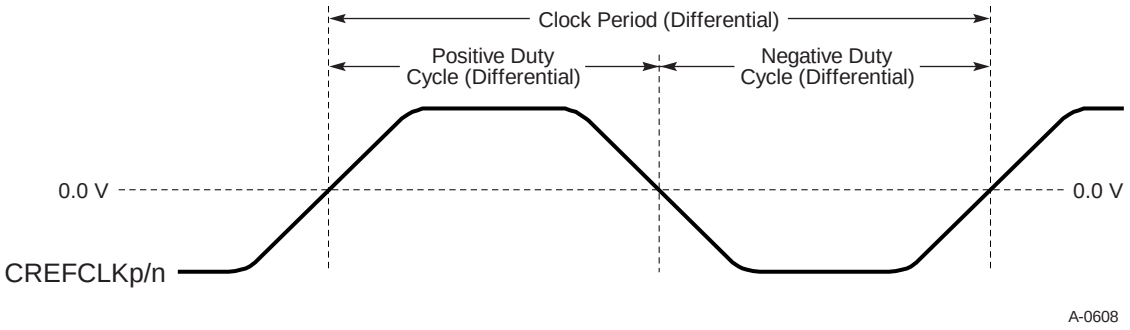


Figure 2-16: Differential Measurement for Duty Cycle and Period

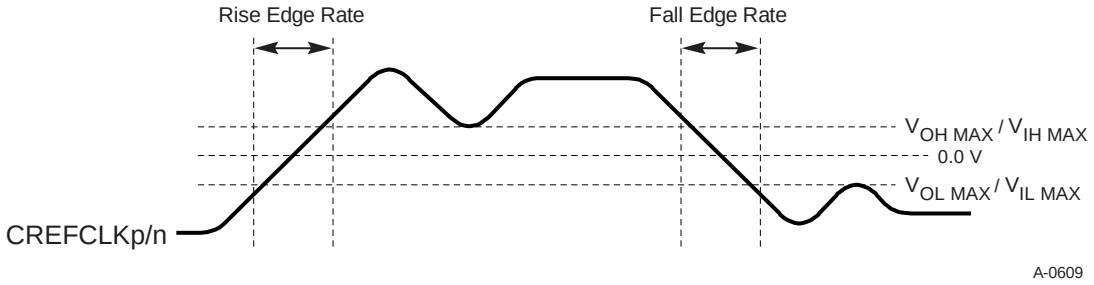


Figure 2-17: Differential Measurement Points for Rise and Fall Time

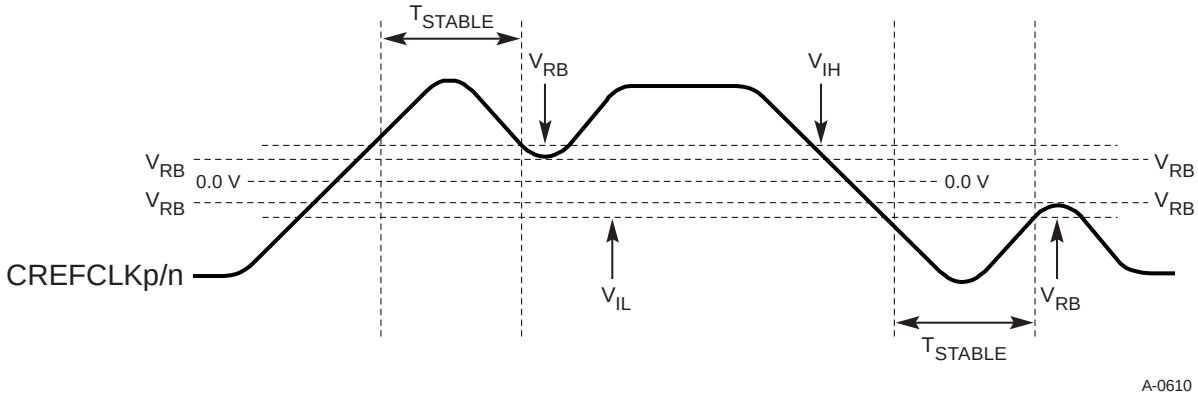


Figure 2-18: Differential Measurement Points for Ringback

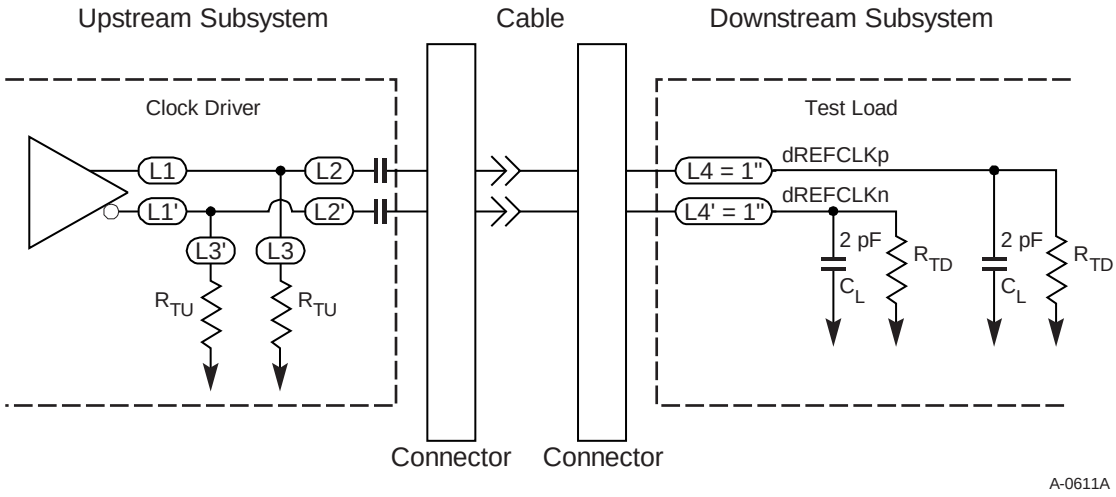


Figure 2-19: CREFCLK Measurement and Test Load

In the case of a Subsystem containing multiple external cable interfaces, the reference-clock pair is routed point-to-point to each cable connector. The phase relationships of the clocks to the connectors are not specified; however, clock skew between an Upstream Port and its corresponding CREFCLK shall adhere to the $t_{CLK\text{-}SKEW}$ timing parameter as specified in Table 2-3 and described further in Section 2.3.5. The clocks shall be routed according to best-known differential clock routing rules.

2.12.4. Phase Jitter

2.5 GT/s

Maximum jitter contribution resulting from the reference clock circuit has been specified by the *PCI Express Card Electromechanical Specification, Revision 1.1*. Although the limits for jitter contribution from cabled PCI Express applications fall outside those set for desktop form factors, the same test and measurement philosophy is utilized. Cable reference clock phase jitter measurements are taken at the cable connector of the Upstream Subsystem using the circuit shown in Figure 2-19.

Eye closure resulting from the phase jitter content on CREFCLK is measured to be the same as other PCI Express form factor requirements. It should be noted that, due the increased round-trip delay of the interconnect, additional jitter budget is to be allocated to the CREFCLK. Section 3.2.3.2 specifies the actual jitter budget breakdown for cabled applications based on a roundtrip delay of 70 ns.

Refer to the *PCI Express Card Electromechanical Specification, Revision 1.1* for additional details on the reference clock phase jitter requirements and measurement thereof.

5.0 GT/s

The phase jitter analysis method for 5.0 GT/s follows the same general test methodology as the *PCI Express Base Specification, Revision 2.0*. The methodology calculates an RMS value and incorporates this amount into the link jitter budget as a Random Jitter component. Cable reference clock phase jitter measurements are taken at the cable connector of the upstream subsystem using the circuit shown in Figure 2-19.

The round trip delay used for the 5.0 GT/s cable implementation is dependent on cable length and electrical properties. The limit for electrical round trip electrical delay is 40 ns. The phase jitter analysis breaks the jitter into its frequency components and certain jitter frequency components increase with the length of the cable, while others decrease Because of this frequency-delay interaction, the round trip delay used in the calculation must be swept from 12 ns to 40 ns to find the maximum jitter. In addition, all combinations of CDR loop filter combinations must be evaluated for each electrical delay value. The sweeps are necessary to analyze the impact of the various combinations of device behavior and possible cable delays. The maximum value must be used to determine if the CREFCLK complies with the value specified in Table 2-4. Note: If the transfer function characteristics of the devices at one or both ends are known, then the clocking analysis may limit the REFCLK transfer function combinations used in the analysis. Analysis should be performed according to the analysis techniques described in the *PCI Express Base Specification, Revision 2.0*.

OBSERVATION: The filter functions for REFCLK jitter analysis must be swept across the required transport delay range to find the worst case RMS jitter value. Based on testing, a 6 ns round trip resolution has been shown to locate the region of the region where jitter peaks. Finer resolution should be used in this region to find the specific delay where the maximum jitter value occurs.

The jitter for the cabled link will likely be tighter than that for the *PCI Express Card Electromechanical Specification, Revision 2.0*. The implication is that a host provided reference clock for a cabled link may not meet the timing requirements when evaluated across phase delays longer than the 12 ns used in the CEM analysis. Additional steps to guarantee a compliant clock source may be required.

3

3. PCI Express Signals

Each PCI Express Lane consists of a pair of differential signals. The Transmitter pair is labeled PETpN and PETnN where N is the lane number (starting with 0); "p" is the true signal while "n" is the complement signal. The Transmitter pair originating in the Upstream Subsystem is connected to a Receiver pair at the Downstream Subsystem at the opposite side of the cable. The Receiver pair is labeled PERpN and PERnN with the same labeling convention as the Transmitter pair.

Support for Polarity Inversion is required on all PCI Express Receivers across all Lanes independently. The "p" and "n" connections may be reversed to simplify trace routing and minimize vias if needed. All PCI Express Receivers incorporate automatic Polarity Inversion as part of the Link Initialization and Training and will correct the polarity independently on each differential pair. Refer to Chapter 4 of the *PCI Express Base Specification*.

Support for Lane Reversal is optional. An example of Lane Reversal consists of Lane 0 of an Upstream Port attached to Lane N-1 of a Downstream Port where either the Downstream or Upstream device may reverse the Lane order to configure a xN Link. Refer to Chapter 4 of the *PCI Express Base Specification*.

A null modem function for connecting the transmit pair on one side to the receive pair to the other side is performed within the cable assembly. External cable connector pin assignments are identical at both sides of the Link. Lane Polarity Inversion and/or Lane reversal shall not be implemented within the cable assembly.

One exception exists where the pin assignments are not identical at both sides of the Link. In the case of the x16 cable assembly, the sideband signals are at different locations to simplify manufacturing of the cable assembly.

Support of Low-Power PCI Express signaling, without de-emphasis, as specified by the *PCI Express Base Specification* and the *PCI Express Mobile Graphics Low-Power Addendum to the PCI Express Base Specification* is outside the scope of this specification.

3.1. Interconnect

In the context of this specification, the interconnect comprises of everything between the pins of a Transmitter package and the pins of a Receiver package. This consists of traces on printed circuit boards, cable, AC-coupling capacitors, and connectors. The interconnect total capacitance to ground seen by the Receiver Detection circuit (see Chapter 4 of the *PCI Express Base Specification*) shall not exceed 3 nF**,** including capacitance added by attached test instrumentation. Note that this capacitance is separate and distinct from the AC-coupling capacitance value (see Section 3.2.1).

3.1.1. Link Definition

Typical cabled PCI Express Links, from source to destination, consist of the following:

- Transmitters on an ASIC on a printed circuit board
- Package fan-in-out trace topologies
- PCB coupled microstrip and/or stripline traces
- AC-coupling capacitors
- Vias for layer changes
- Cable mated connector
- External raw cable
- Cable mated connector
- Coupled microstrip line and/or stripline traces
- Package fan-in-out trace topologies
- Receivers on an ASIC on a printed circuit board

The electrical parameters for the Link are subdivided into three components, as identified by the dashed lines in Figure 3-1. Note that for validation purposes, the separation is somewhat different to facilitate ease of connecting any test and measurement equipment.

- Upstream Subsystem
- Cable including mated connectors
- Downstream Subsystem

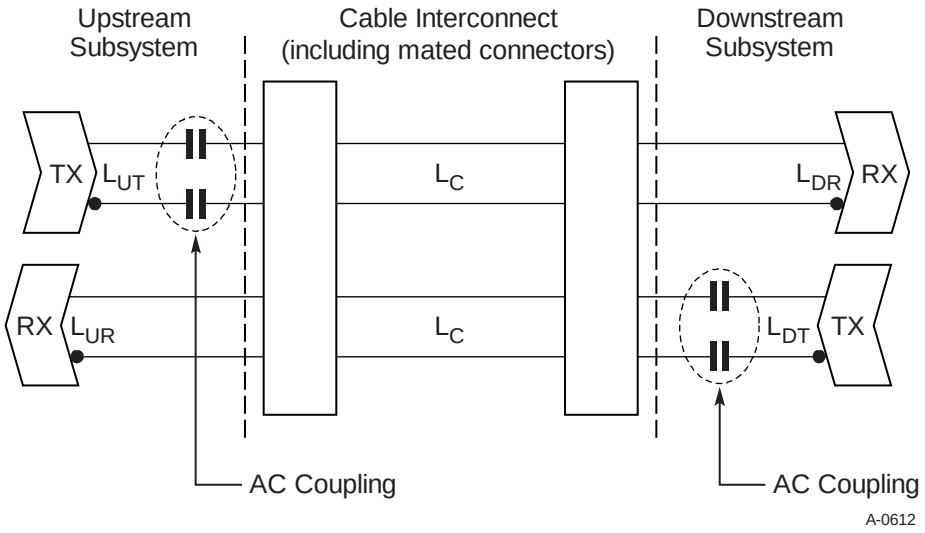


Figure 3-1: Electrical Parameter Allocation

3.2. Electrical Budgets

A budget is incorporated for each of the following electrical parameters associated with the Link:

- AC-coupling capacitors
- Insertion Loss (Voltage Transfer Function)
- Jitter
- Bit-to-bit skew
- Crosstalk
- Transmitter de-emphasis
- Skew within a differential pair

The electrical budgets are different for two of the three Link components:

- Upstream/Downstream Subsystem
- Cable budget, including mated connectors and their footprints

The Subsystem's budget allocations associated with the Transmitters and Receivers differ. This is to account for any electrical characteristics the AC-coupling capacitors may contribute to the Link.

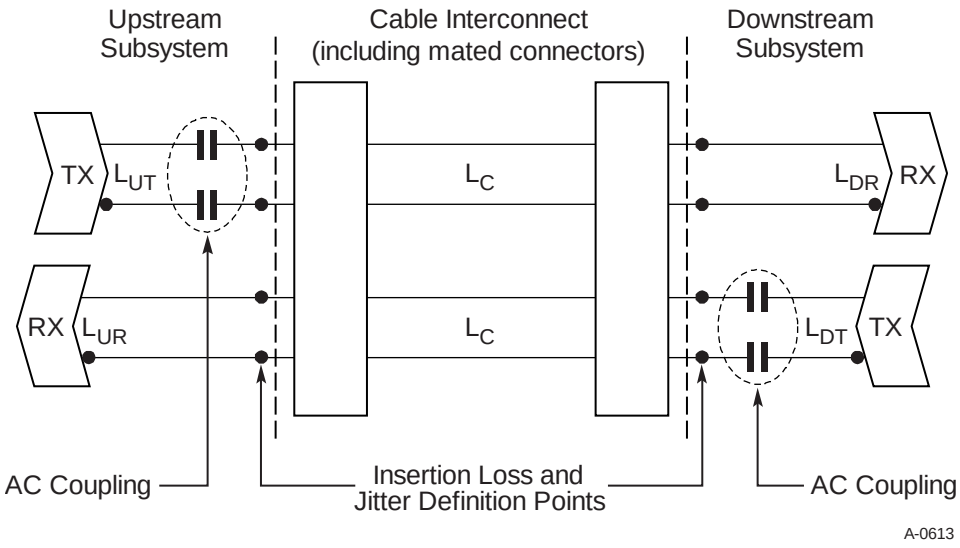


Figure 3-2: Loss and Jitter Definition Points

3.2.1. AC-coupling

AC-coupling is required at the Transmitter (see Figure 3-2) with values as specified in Chapter 4 of the *PCI Express Base Specification*.

3.2.2. Insertion Loss

Insertion loss budgets as specified in Table 3-1 and Table 3-2 are provided as guidance for product development. The total available loss budget, in frequency domain decibels (dB), has been divided among the three segments (Upstream Subsystem, cable, and Downstream Subsystem) as depicted in Figure 3-2. Subsystem compliance testing shall be performed against the eye diagrams specified in Section 3.3. Cable assembly compliance requirements are provided in Chapter 6.

The maximum loss in dB (frequency domain decibels) is specified for the Subsystem boards and the cable. The insertion loss values for a Subsystem are defined as the ratio of the voltage at the ASIC package pin and the voltage at the PCI Express cable connector interface, terminated by 100 Ω differentially, realized as two 50 Ω resistances. These resistances are referenced to ground at the connector footprint. Mated connectors, and their foot print for mounting to a printed circuit board, are not included within the Subsystem budgets.

The maximum loss in dB for the cable is defined as the ratio of the source voltage at one end of the cable and the output voltage, terminated by 100 Ω differential termination, realized as two 50 Ω resistances, at the other end. The cable loss budget includes mated connectors at both ends and their footprints.

Table 3-1: 2.5 GT/s Insertion Loss Budget Allocation

Loss Parameter	Symbol	Insertion Loss at 1.25 GHz (dB)	Insertion Loss at 625 MHz (dB)	Notes
Total Loss	L_{Total}	< 10.75	< 6.80	1
Upstream Subsystem	L_{UT}	< 1.75	< 1.00	2, 3, 4
	L_{UR}	< 1.50	< 0.80	2, 4
Cable and Connectors	L_C	< 7.50	< 5.00	2
Downstream Subsystem	L_{DT}	< 1.75	< 1.00	2, 3, 4
	L_{DR}	< 1.50	< 0.80	2, 4

Table 3-2: 5.0 GT/s Insertion Loss Budget Allocation

Loss Parameter	Symbol	Insertion Loss at 2.5 GHz (dB)	Insertion Loss at 1.25 MHz (dB)	Notes
Total Loss	L_{Total}	< 13.6	< 8.5	1
Upstream Subsystem	L_{UT}	< 2.2	< 1.3	2, 3, 4, 5
	L_{UR}	< 2.1	< 1.3	
Cable and Connectors	L_C	< 9.3	< 5.9	2, 6
Downstream Subsystem	L_{DT}	< 2.2	< 1.3	2, 3, 4, 5
	L_{DR}	< 2.1	< 1.3	

Notes:

1. The interconnect insertion loss values given in Table 3-1 and the cable assembly differential characteristics given in Section 6.2.2 are specified to insure that the interconnect jitter budget and the insertion loss allocation for the interconnect *PCI Express Base Specification* operational loss budget are met. The insertion loss values in Table 3-1 and the insertion loss values determined using Equation (6-1) represent the insertion loss at a given frequency expressed in (dB). The operational loss budget in the *PCI Express Base Specification* is calculated as the ratio of voltages expressed in dB (e.g., 13.2 dB at 1.25 GHz). Although both values are expressed in units of dB, the quantities used in the ratios are not common; therefore, the results cannot be added or subtracted directly. The values given in Table 3-1 and the cable assembly differential characteristics given in Section 6.2.2 account for the eye closure due to ISI, return loss, and crosstalk.
2. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver, respectively and C, U, and D represent the cable assembly and Upstream and Downstream Subsystem, respectively. The cable and connector loss includes both mated connectors including their footprints (pad size, anti-pad construction, and parasitic capacitance).
3. Including AC coupling capacitor loss.
4. No specific trace geometry is explicitly defined in this specification for the interconnect Subsystem loss. Tradeoffs between laminate quality, via count, impedance mismatch, and crosstalk can be implemented within the limits specified.
5. Including AC coupling capacitor pad loss. The capacitor response is not included.
6. The values for the cable assembly are stated in Table 6-18.

3.2.3. Jitter Budgets

The maximum jitter values in terms of percentage of Unit Interval (UI = 400 ps for 2.5 GT/s and 200 ps for 5.0 GT/s) are specified for the Subsystems and the cable including mated connectors. The jitter values are defined with respect to 100 Ω differential termination, realized as two 50 Ω resistances. These resistances are referenced to ground at the definition points, as depicted in Figure 3-2.

Aside from the Transmitter, Receiver, and Interconnect jitter budgets, some portion of the UI is reserved for phase jitter introduced by the reference clock generator. This specification builds upon the *PCI Express Base Specification, Revision 1.1*, and *Card Electromechanical, Revision 1.1* specifications for 2.5 GT/s and *PCI Express Base Specification, Revision 2.0* for 5.0 GT/s, which provide clock generator and PCI Express transceiver requirements. Refer to Section 2.12.4 and the respective white papers available from the PCI-SIG for additional details on the impact of phase jitter on eye closure.

3.2.3.1. Random Jitter (Rj)

The *PCI Express Base Specification* provides the budget for Total Jitter (Tj) at a Bit Error Ratio (BER) of 10^{-12} for 2.5 GT/s. This does not make any assumption or quantification of Random Jitter (Rj). However, for 5.0 GT/s, random jitter components are defined in the jitter modeling. This cable specification includes assumptions for an overall system budget of Rj and calculates the eye openings appropriately for a measurement specification using a sample size of 10^6, extrapolated to a 10^{-12} BER. The convolution of the Rj term provides sufficient specification relief so that the addition of the reference clock jitter term does not exceed the entire system budget.

The Rj assumptions are taken to be conservative "in system" minimum Rj numbers. A device manufacturer that does not have a minimum Rj component would need to appropriately adjust the Deterministic Jitter (Dj) of the component to compensate.

3.2.3.2. System Level Jitter Distribution

The total system jitter budget is derived with the assumption of a minimum Rj for each of the four budget items. This minimum Rj component is used to determine the overall system budget. The probability distribution of the Rj component is at the Bit Error Ratio (BER) indicated and Gaussian.

For any jitter distribution, the Tj shall always be met at the BER. Tradeoffs of Rj and Dj are allowed, provided the Tj, as defined in Table 3-3 and Table 3-4, are always met. The Rj of the components are independent and convolve as the root sum square.

Table 3-3: Total System Jitter Distribution at 2.5 GT/s

Jitter Contribution	Max Rj (ps) RMS	Dj (ps) Peak-to-Peak	Tj at BER 10^{-12} (ps)	Tj at 10^6 Samples (ps)
Transmitter	2.8	60.6	100	87
Reference Clock[1,2]	4.7	61.9	128	106
Interconnect	0	70	70	70
Receiver	2.8	120.6	160	147
Linear Total Tj:			458	410
Root Sum Square (RSS) Total Tj:			399.13	371.52

Table 3-4: Total System Jitter Distribution at 5.0 GT/s

Jitter Contribution	Max Rj (ps) RMS	Dj (ps) Peak-to-Peak	Tj at BER 10^{-12} (ps)	Tj at 10^6 Samples (ps)
Transmitter	1.4	30	49.7	43.3
Reference Clock[1,2]	3.1	0	43.6	29.5
Interconnect	0	58	58	58
Receiver	1.4	60	79.7	73.3
Linear Total Tj:			231	204
Root Sum Square (RSS) Total Tj:			199.75	182.97

Notes:

1. Long roundtrip delay from external cables has a negative impact on eye closure resulting from CREFCLK phase jitter. This specification divides the jitter budget to accommodate for the impact of a 40 ns roundtrip delay from the interconnect.

2. RSS equation for BER 10^{-12}: Tj = $\sum Dj_n$ + 14.069 * $\sqrt{\sum Rj_n^2}$

3. RSS equation for 10^6 samples: Tj = $\sum Dj_n$ + 9.507 * $\sqrt{\sum Rj_n^2}$

4. The base specification calculates the RMS Jitter of the reference clock in a system operating at 5.0 GT/s. This is then treated as a random jitter component when creating total jitter for the link jitter budget calculation at 5.0 GT/s. The Card Electromechanical specification breaks the reference clock jitter into specific random and deterministic jitter components when analyzing the link jitter budget for 2.5 GT/s. Refer to Section 4.6.7 of the *PCI Express Base Specification, Rev. 2.0* for the limits of reference clock jitter for operation at 5.0 GT/s and the Card Electromechanical Specification for the limits of the reference clock jitter when operating at 2.5 GT/s.

3.2.4. Interconnect Jitter Budget Allocation

The maximum jitter values in terms of percentage of Unit Interval are specified for the Subsystems and the cable. The jitter values are defined with respect to 100 Ω differential termination, realized as two 50 Ω resistances. These resistances are referenced to ground at the measurement point, as depicted in Figure 3-2.

Section 3.2.3 provides information on jitter budget allocation for the complete Link, including that for the Transmitter, Receiver, and reference clock. The available 58 ps interconnect jitter budget is divided over the Subsystems and cable assembly.

Data Dependent Jitter (DDJ), resulting from inter-symbol interference (ISI), increases at an accelerated rate for cable lengths exceeding 5 meters. The jitter levels are dependent on the wire gauge employed and the actual de-emphasis level driven from the PCI Express component. Controlling the ISI jitter component through additional equalization within the cable assembly is allowed. Details of such implementations are beyond the scope of this specification.

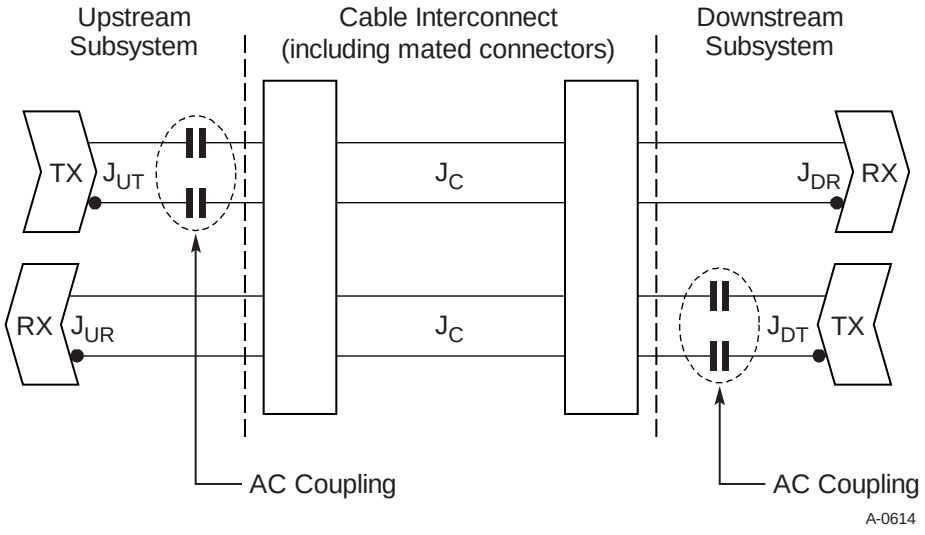


Figure 3-3: Jitter Budget Allocation

Table 3-5: Interconnect Jitter Budget at 2.5 GT/s

Jitter Parameter	Peak-to-Peak Jitter Budget Value UI (ps)		Notes
Upstream Subsystem	J_{UR} < 0.020 (8 ps)	J_{UT} < 0.010 (4 ps)	1, 2, 3
Cable and Mated Connectors	J_C < 0.145 (58 ps)	J_C < 0.145 (58 ps)	1, 4
Downstream Subsystem	J_{DT} < 0.010 (4 ps)	J_{DR} < 0.020 (8 ps)	1, 2, 3
Total Jitter	J_{Total} < 0.175 (70 ps)		1, 5

Table 3-6: Interconnect Jitter Budget at 5.0 GT/s

Jitter Parameter	Peak-to-Peak Jitter Budget Value UI (ps)	Notes
Transmitter Subsystem	< 0.035 (7 ps)	1, 2, 3
Cable and Mated Connectors	< 0.185 (37 ps)	1, 4
Receiver Subsystem	< 0.07 (14 ps)	1, 2, 3
Total Jitter	0.29 (58 ps)	5

Notes:

1. All values are referenced to 100 Ω, realized as two 50 Ω resistances. The jitter budget values include all possible crosstalk impacts (near-end and far-end), potential mismatch of the actual interconnects with respect to the 100 Ω reference load, and ISI.
2. Jitter is measured at the zero crossings of differential voltage of the compliance pattern, as specified by the *PCI Express Base Specification*, while simultaneously transmitting on all physical Lanes. Jitter budgets assume a standard PCI Express signal source including -6.0 dB (±0.5 dB) of de-emphasis. No guard band is included within the jitter budgets.
3. All values are referenced to 100 Ω. The Transmitter budget includes AC-coupling capacitors and Subsystem interconnect. No specific trace geometry is explicitly defined in this specification.
4. The cable jitter budget includes both mated connectors and the physical cable. The jitter budget distributions in Table 3-5 and Table 3-6 are used to derive the eye diagram widths as described in Section 3.3. Compliance measurements shall be verified against the eye diagrams.
5. Due to the lossy nature of the cabled link, it is unlikely that the maximum allowable jitter will be reached. The link will be loss limited, not jitter limited. However, moving jitter allocations to subsystems will cause the eye to further close due to the nature of the finite rise time and shifting the position of the rising/falling edges due to additional jitter.

3.2.5. Crosstalk

All Subsystem designs shall properly account for any crosstalk that may exist among the various differential signal pairs and other signals alike. Crosstalk may be either near-end (NEXT) or far-end (FEXT). Each crosstalk component can have potential impact on a design and shall be planned for accordingly. Jitter budgets assigned to the Subsystems are set at an absolute minimum to preserve the maximum possible budget for the copper cable interconnect.

Crosstalk between differential pairs on the interconnect will influence and impact the data signals, and any subsequent loss and jitter budgets, as noted in Sections 3.2.2 and 3.2.4. Note that the eye diagrams in Section 3.3 account for any and all crosstalk allowed.

3.2.6. Lane-to-Lane Skew

The skew at any point is measured at the zero crossings of differential voltage of the compliance pattern, while simultaneously transmitting on all Lanes. The compliance pattern is defined in the *PCI Express Base Specification*.

Table 3-7: Allowable Interconnect Lane-to-Lane Skew

Skew Parameter	Symbol	Skew Values	Comments
Total Interconnect Skew	S_T	2.0 ns	This does not include Transmitter output skew
Subsystem	S_S	0.35 ns	
Cable	S_C	1.30 ns	

3.2.7. Transmitter De-Emphasis

De-emphasis is required in the Transmitter to reduce ISI. Per Chapter 4 in the *PCI Express Base Specification*, this is implemented as a -3.5 dB (±0.5 dB) attenuation of all non-transition bits relative to the amplitude of the preceding transition bit when operating at 2.5 GT/s. For 5.0 GT/s, the *PCI Express Base Specification, Revision 2.0* adds an additional setting of -6.0 dB (+/- 0.5 dB). For the cabled implementation, transmitters shall be configured for the -6.0 dB de-emphasis setting. While not optimal for all cable lengths, sufficient margin exists when using low-loss cables for reliable operation with the -6.0 dB setting.

3.2.8. Skew Within the Differential Pair (Intra-Pair Skew)

Skew within a differential pair (intra-pair skew) gives rise to a common-mode signal component, which can, in turn, increase Electromagnetic Interference (EMI). The differential pair(s) on a Subsystem printed circuit board should be routed such that the skew within each differential pair is ≤0.005 inch.

Intra-pair skew of the cable assembly is more difficult to control and tight specifications result in increased cost. A maximum skew of 0.2 UI is recommended for the cable assembly intended to

operate at 2.5 GT/s. It is left up to the application to make appropriate cost/performance tradeoffs. No specific budgets are provided for intra-pair skew of the cable assembly as these are incorporated within the overall cable assembly budgets.

For 5.0 GT/s, skew is not explicitly defined for the cable. Instead, a limit is placed on mode conversion for the cable assembly in Section 6.2.2.10.

3.3. Eye Diagrams

The eye diagrams defined in this section represent the compliance eye diagrams that shall be met for both Upstream and Downstream Subsystems. Transceiver silicon requirements are as specified in the *PCI Express Base Specification*.

3.3.1. Transmitter Compliance Eye

The Transmitter compliance eye is defined by the values in Table 3-8 and Table 3-9 and Figure 3-4.

Table 3-8: Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Value	Notes
Vtx_A	≥ 654 mV	1, 2, 4, 5
Vtx_A_d	≥ 450 mV	1, 2, 4
Ttx_A @ BER 10^{-12}	≥ 296 ps	1, 3, 4
Ttx_A @ 10^6 Samples	≥ 309 ps	1, 3, 4

Table 3-9: Transmitter Path Compliance Eye Requirements at 5.0 GT/s

Parameter	Value	Notes
Vtx_A	≥ 612 mV	1, 2, 4, 5, 6
Vtx_A_d	≥ 369 mV	1, 2, 4, 6
Ttx_A @ BER 10^{-12}	≥ 149 ps	1, 3, 4, 6
Ttx_A @ 10^6 samples	≥ 148 ps	1, 3, 4, 6

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
2. Transition and non-Transition bits shall be distinguished in order to measure compliance against the de-emphasized voltage level (Vtx_A_d).
3. Ttx_A is the eye width.
4. The values in Table 3-8 and Table 3-9 are referenced to an ideal 100 Ω differential load, at the end of the interconnect path being tested, at the connector boundary on the Subsystem. This ideal 100 Ω differential load is implemented as two 50 Ω resistors to ground. The eye diagram is defined and centered with respect to the jitter median.
5. Maximum differential output voltage is 1.2 V as specified by the *PCI Express Base Specification.*

6. Transition bits measured with transmitter set to -6.0 dB of de-emphasis. Transition and non-Transition bits shall be distinguished in order to measure compliance against the de-emphasized voltage level (Vtx_A_d).

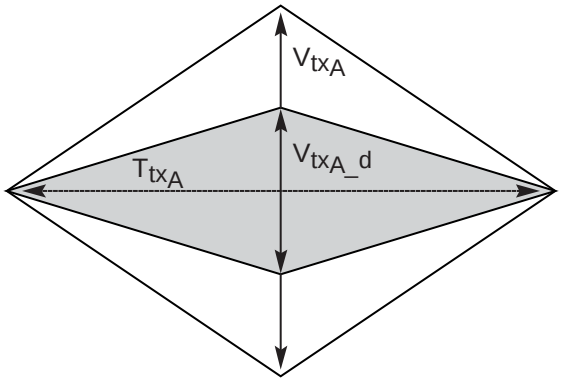


Figure 3-4: Transmitter Compliance Eye

3.3.2. Receiver Compliance Eye

The minimum sensitivity for the Subsystem's Receiver path compliance is specified in Table 3-10 for 2.5 GT/s and Table 3-11 for 5.0 GT/s, and a representative eye diagram is shown in Figure 3-5.

Table 3-10: Receiver Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Value	Notes
Vrx_A	≥ 208 mV	1, 2, 3, 5, 6
Vrx_A_d	≥ 192 mV	1, 2, 3, 5
Trx_A @ BER 10^{-12}	≥ 234 ps	1, 2, 4, 5
Trx_A @ 10^6 Samples	≥ 247 ps	1, 2, 4, 5

Table 3-11: Receiver Path Compliance Eye Requirements at 5.0 GT/s

Parameter	Value	Notes
Vrx_A	>203 mV	1, 2, 3, 5, 6
Vrx_A_d	≥ 203 mV	1, 2, 3, 5
Trx_A @ BER 10^{-12}	≥ 122 ps	1, 2, 4, 5
Trx_A @ 10^6 samples	≥ 127 ps	1, 2, 4, 5

Notes:

1. All signal and timing values are referenced at the Subsystem connector mounting pads.
2. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
3. Transition and non-Transition bits shall be distinguished in order to measure compliance against the de-emphasized voltage level (Vrx_A_d).

4. Trx_A is the eye width.
5. The values in Table 3-10 and Table 3-11 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the connector boundary on the Subsystem. This ideal 100 Ω differential load is implemented as two 50 Ω resistors to ground. The resultant values, when provided to the Receiver interconnect path of the Subsystem, allow for a demonstration of compliance of the overall Subsystem's Receiver path. The sensitivity requirements are defined and centered with respect to the jitter median.
6. Maximum differential input voltage is 1.2 V as specified by the *PCI Express Base Specification.*

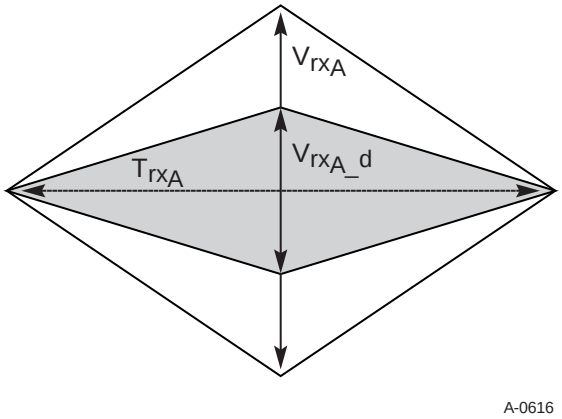


Figure 3-5: Receiver Compliance Eye

3.4. ESD

PCI-express cable ports of all link widths shall withstand 2 kV of ESD contact discharge to the connector cage using the human body model (HBM), Class 2 per JEDEC JESD 22-A114:B 2000 with power applied, without damage not limited to latch up, without a cable attached, and without non-recoverable errors with a cable attached.

A recoverable error is one that does not require reset or replacement of the device.

3.5. Link Power Management

The *PCI Express Base Specification* specifies Link Power Management states, some of which are required by all existing form factor specifications while others may be optional. A cabled PCI Express Port, adhering to this specification, may be implemented on top of any other form factor. Support of Link Power Management states are considered to be a system level requirement and are not imposed by this specification.

Downstream Subsystems should support all defined Link Power Management states to guarantee compliancy with system level specifications.

Support for dynamic control of CREFCLK during L1 Power Management states, using the CLKREQ# protocol as described in the *PCI Express Base Specification* and the *ExpressCard Standard*, is not provided by this specification.

4

4. Cable Interoperability

4.1. Cable Connector Identification

Identification of cable purpose is accomplished by means of marking on the cable connector; e.g., "PCIe x4" and "PCIe x8."

Although there are different configurations that potentially do not interoperate, a mechanical feature exists to minimize the potential of inserting smaller cable connectors into larger openings.

4.2. Cable Length

Cable length targets and limitations are intentionally not imposed by this specification. It should be noted that extended cables are more sensitive to a variety of factors. Following are some potential limitations that could limit the maximum supported cable length. It is beyond the scope of this specification to address potential issues that might arise from such application requirements.

- PCI Express signaling is not suited for driving very long cables. Cable assembly and Subsystem loss and jitter budgets are derived based on PCI Express parameters as defined within the *PCI Express Base Specification, Revision 2.0*. Any application going beyond the budgets provided within this cable specification, either a Subsystem or cable assembly, is not guaranteed to interoperate.
- PCI Express protocol parameters might need to be evaluated against packet flight and acknowledgement time of the cabled Link: essentially the round trip delay. The PCI Express protocol is based on credits and includes time dependent control functions such as a replay-timer. Any such time dependency could affect obtainable bandwidth or worse.
- Phase jitter impact from the reference clock increases with longer cable delays, thus decreases the PCI Express electrical budgets available to Link. Budget allocation, as provided within this cable specification, has chosen a maximum round-trip delay of 70 ns for 2.5 GT/s and 66 ns for 5.0 GT/s. This is roughly equivalent to the longest cable that can be achieved, from an insertion loss perspective, using PCI Express signaling and 24 AWG wire. Any attempt to obtain a larger round-trip delay (longer cables) requires jitter budget tradeoffs to be made or an alternate clocking architecture. To maintain compatibility with the 2.5 GT/s standard, cable lengths will not be increased by this specification.
- Certain sideband signal timing and level parameters might be violated depending on cable length and type.

4.3. Cable Assembly Configuration

Cable assemblies are to contain a single Upstream connection and a single Downstream connection. The concept of a split-endpoint cable is beyond the scope of this specification.

5

5. Connector Definition

This document defines distinct connectors to support four different link widths: x1, x4, x8, and x16. One cable connector is defined for each of these four Link widths. A low cost x2 connector may be defined in a future specification revision. All electrical and mechanical testing to be conducted in compliance with EIA-364.

5.1. Signal Description

The external PCI Express cable connector and cabling support the following signals:

- PETpN/PETnN (required): PCI Express Transmitter pair(s), labeled where N is the Lane number (starting with 0); "p" is the true signal while "n" is the complement signal.
- PERpN/PERnN (required): PCI Express Receiver pair(s), labeled where N is the Lane number (starting with 0); "p" is the true signal while "n" is the complement signal.
- Auxiliary signals as defined in Chapter 2.

5.2. x1 Connector Definition

5.2.1. Pin-out (x1)

Table 5-1: x1 Connector Pin Assignment

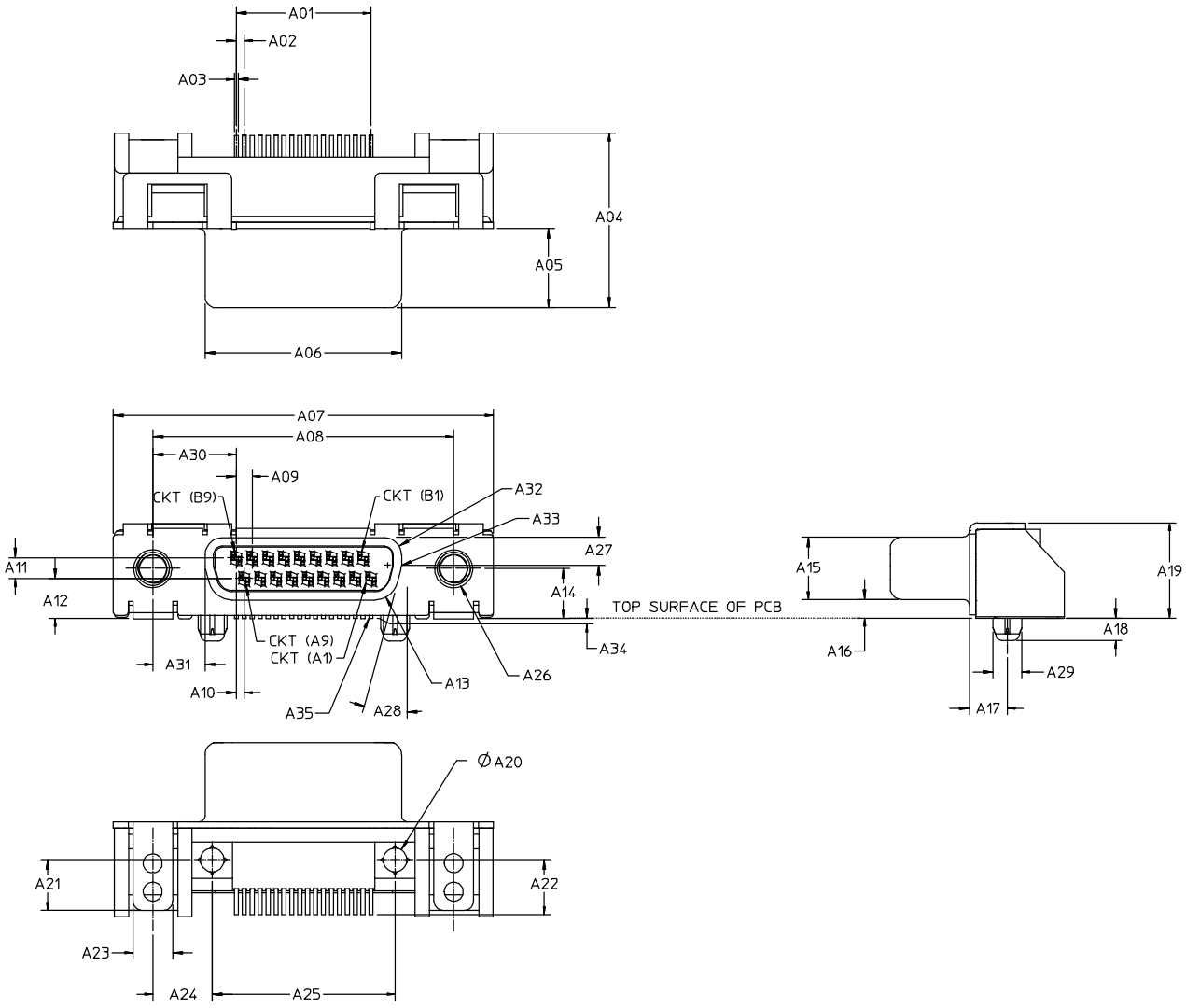
Pin#	Signal	Description	Notes
A1	PERn0	Differential PCI Express Receiver Lane	5
A2	PERp0		
A3	RSVD	Reserved	2
A4	SB_RTN	Signal Return for Single Ended Sideband Signals	
A5	CREFCLKn	Differential 100 MHz Cable Reference Clock	
A6	CREFCLKp		
A7	PWR_RTN	Return for +3.3 V Power (Optional)	4
A8	CPERST#	Cable PERST#	
A9	GND	Ground Reference for PCI Express Transmitter Lane	
B1	GND	Ground Reference for PCI Express Receiver Lane	

Pin#	Signal	Description	Notes
B2	RSVD	Reserved	2
B3	CWAKE#	Power Management Signal for Wakeup Events (Optional)	1, 3
B4	CPRSNT#	Used for Detection of Whether a Cable is Installed and the Downstream Subsystem is Powered	
B5	GND	Ground Reference for Cable Reference Clock	
B6	PWR	+3.3 V Power (Optional)	1, 4
B7	CPWRON	Upstream Subsystem's Power Valid Notification	
B8	PETn0	Differential PCI Express Transmitter Lane	5
B9	PETp0		

Notes:

1. Optional signals that are not implemented are to be left as no connects on the Board-Side connector.
2. Reserved signals shall be left as no connects on the Board-Side connector.
3. Although support of CWAKE# is optional from the Board-Side connector perspective, an allocated wire is mandated for the cable assembly.
4. These power connections are provided for active circuitry within the cable connector backshell at the ends of the cable and have no conductor within the cable (i.e., these signals do not actually go across the cable).
5. Board-Side pin-out on both sides of the Link is identical. The cable assembly incorporates a null modem for the PCI Express transmit and receive pairs. Polarity Inversion and Lane Reversal shall not be implemented within the cable assembly.

5.2.2. Board-Side Mechanical Drawings



Note:
1. Jackpost thread is to be 4-40 UNC-2A.

Figure 5-1: x1 Board-Side Connector Form Factor

Table 5-2: x1 Board-Side Connector Form Factor Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
A01	First to Last	10.80	Ref
A02	Pitch	0.64	±0.13
A03	SMT Solder Foot Width	0.33	±0.13
A04	OAL Connector	13.97	±0.25
A05	Shell Depth	6.35	±0.13

Designator	Description	Dimension (mm)	Tolerance (mm)
A06	Shell Width	15.87	±0.07
A07	OAW Connector	30.48	±0.25
A08	Jackpost Hole Spacing	24.13	±0.13
A09	Contact Pitch Within Row (Typical)	1.27	±0.13
A10	Contact Pitch Row to Row (Typical)	0.64	±0.13
A11	Contact Height Spacing Between Rows	1.65	±0.13
A12	Ground Tab/Standoff to Bottom Row Contacts	3.19	±0.13
A13	D Shell Lower Radius	1.12	±0.05
A14	Ground Tab/Standoff to Center of Jackpost Hole	4.01	±0.13
A15	D Shell Height	5.07	±0.07
A16	Ground Tab/Standoff to Bottom of D Shell	1.51	±0.13
A17	Peg Location	3.05	±0.13
A18	Peg Height	1.78	±0.13
A19	Ground Tab/Standoff to Top of Connector	7.65	±0.13
A20	Peg Diameter	1.91	±0.13
A21	Center of Peg to End of Ground Tab	4.03	±0.25
A22	Center of Peg to End of SMT Solder Feet	4.40	±0.25
A23	Ground Tab Width	3.18	±0.13
A24	Center of Peg to Center of Ground Tab	4.77	±0.13
A25	Center of Peg to Center of Peg	14.66	±0.13
A26	Internal Threads for Jackpost	4-40	
A27	D Shell Middle Radius Location	2.27	±0.13
A28	Angle on D Shell	15°	±0.5°
A29	Peg Width	2.31	±0.05
A30	Center of Jackscrew Hole to Center of Circuit B9	6.70	±0.05
A31	Center of Jackscrew Hole to Edge of D Shape	4.19	±0.05
A32	D Shell Upper Radius	1.37	±0.05
A33	D Shell Middle Radius	1.93	±0.05
A34	Signal Tail Height	0.00	±0.08
A35	Signal Tail Co-planarity	0.13	

5.2.3. Recommended Footprint

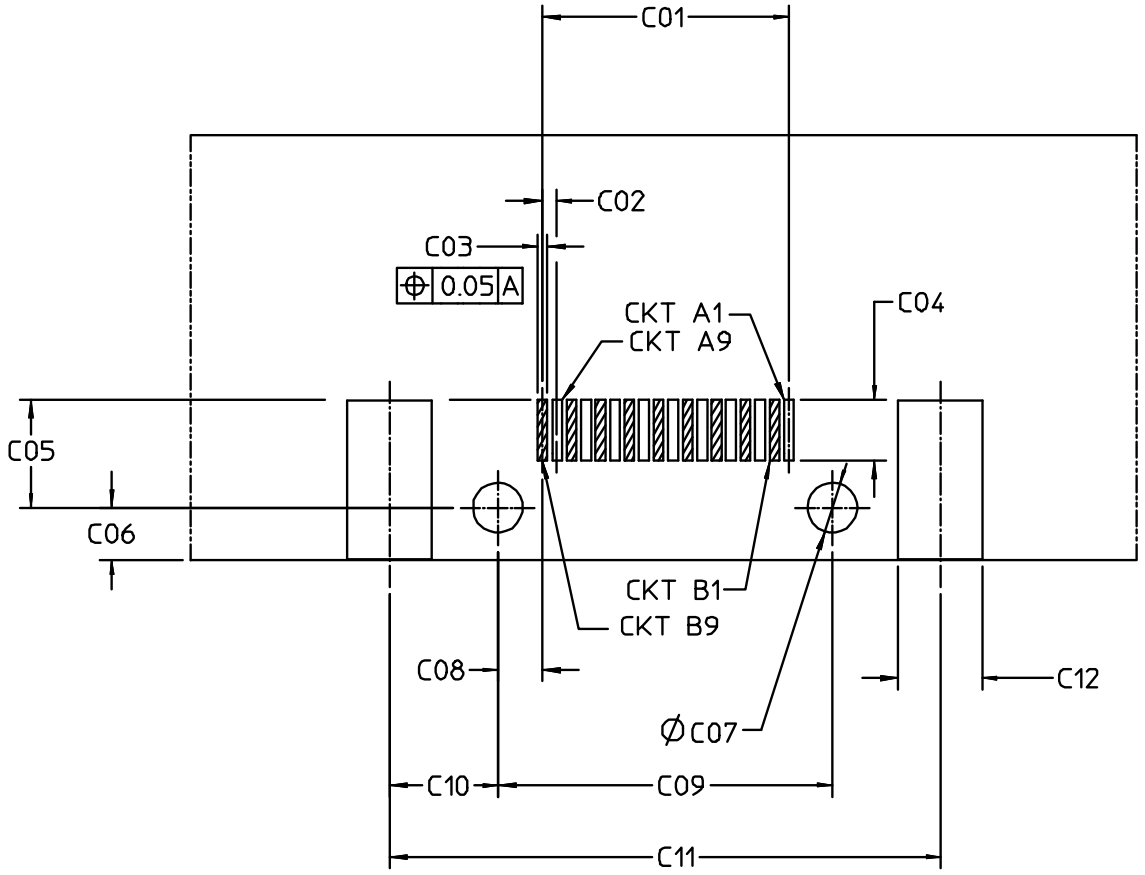


Figure 5-2: x1 Board-Side Recommended Footprint

Table 5-3: x1 Board-Side Recommended Footprint Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
C01	First to Last	10.80	Basic
C02	Pitch Between Solder Pads	0.64	Basic
C03	Solder Pad Width	0.43	±0.03
C04	Solder Pad Length	2.67	±0.13
C05	Center of Hole to End of Solder Pad	4.74	±0.13
C06	From Edge of PCB to Center of Holes	2.29	±0.13
C07	Thru Hole Diameter	2.18	±0.05
C08	Center of Hole to Center of Solder Pad	1.93	±0.13
C09	Center of Thru Hole to Center of Thru Hole	14.66	±0.10

Designator	Description	Dimension (mm)	Tolerance (mm)
C10	Center of Thru Hole to Center of Ground Tab	4.74	±0.13
C11	Center of Ground Tab to Center of Ground Tab	24.13	±0.13
C12	Ground Tab Width	3.68	±0.13

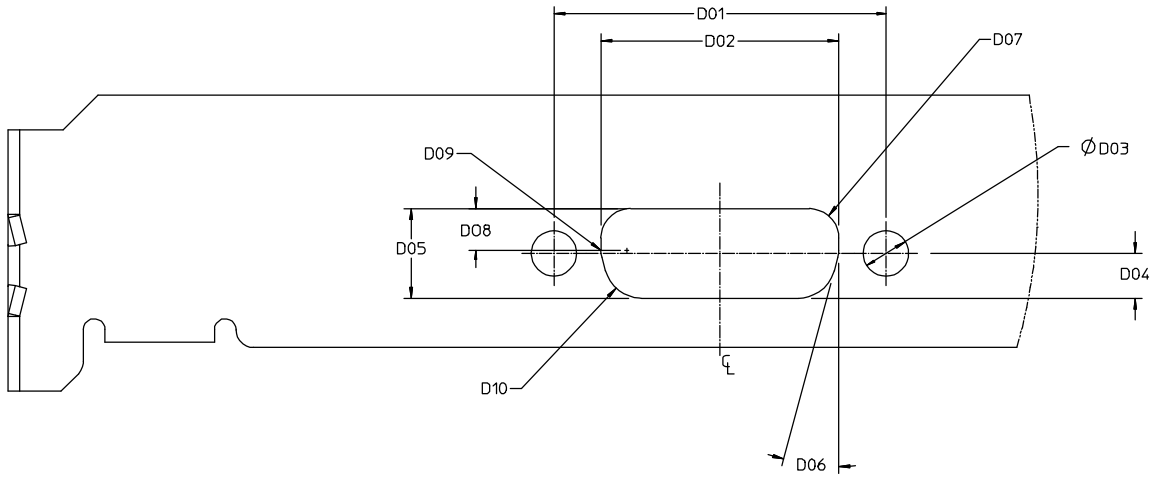


Figure 5-3: x1 Recommended Panel Cut Out

Table 5-4: x1 Recommended Panel Cut Out Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
D01	Center Hole to Center Hole	24.13	±0.13
D02	D Shape Width	17.27	±0.13
D03	Hole Diameter for Jack Post	3.30	±0.13
D04	Bottom of D Shape to Center of Holes	3.26	±0.13
D05	D Shape Height	6.53	±0.13
D06	D Shape Angle	15°	±0.5°
D07	Upper Radius on D Shape	2.13	±0.13
D08	Middle Radius Location	3.03	±0.13
D09	Middle Radius on D Shape	1.88	±0.13
D10	Lower Radius on D Shape	2.69	±0.13

Note:

Although shielding is provided with the connector, in order to meet FCC requirements, gasketing may be required.

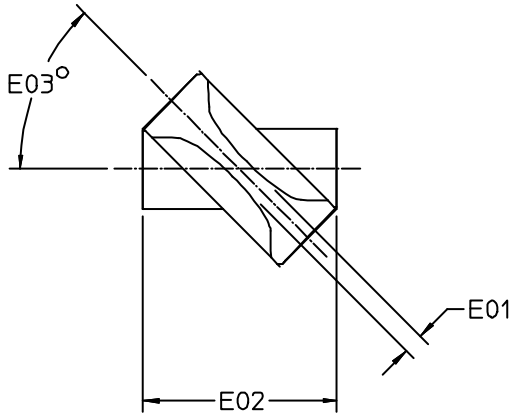


Figure 5-4: x1 Plug Terminal Tip Geometry

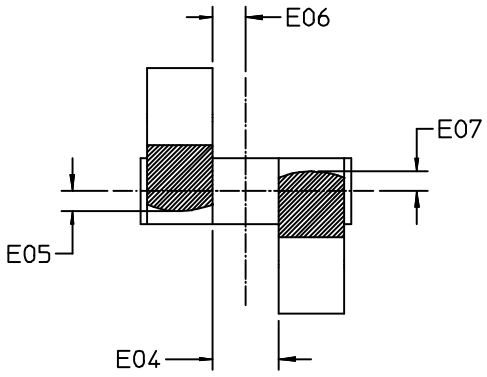
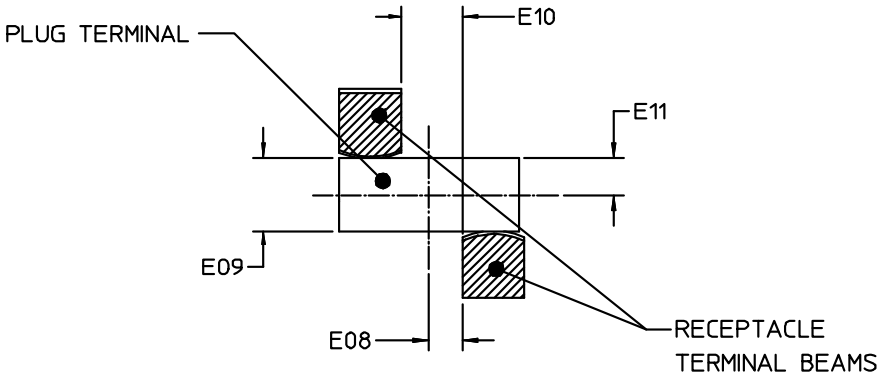


Figure 5-5: x1 Receptacle Terminal Tip Geometry



NOTE: MATED CROSS SECTION IS LOCATED 1.04 AWAY FROM THE FRONT FACE OF THE RECEPTACLE HOUSING AND INCLUDES 0.38 OF FULL CONTACT WIPE.

Figure 5-6: x1 Mated Interface Geometry

Table 5-5: x1 Interface Geometry Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
E01	Plug Beam Lead-in Width	0.08	Maximum
E02	Plug Beam Width	0.69	Minimum
E03	Angle of Plug Beam Twist	45°	±0.5°
E04	Gap Between Contact Beams	0.20	Minimum
E05	Height from Center of Receptacle to Contact Beam	0.11	Maximum
E06	Center of Receptacle to Contact Beam	0.10	Minimum
E07	Height from Center of Receptacle to Contact Beam	0.11	Maximum
E08	Center of Plug Beam to Edge of Contact Beam	0.15	Maximum
E09	Height of Plug Beam	0.28	Minimum
E10	Gap Between Contact Beams When Mated to Plug	0.30	Maximum
E11	Height from Center of Plug to Contact Beam	0.14	Minimum

5.2.4. Electrical Requirements

Table 5-6 lists the electrical performance requirements for PCI Express x1 mated board and cable connectors.

Table 5-6: x1 Connector Electrical Performance Requirements

Symbol	Parameter	Min	Max	Units	Conditions/Comments
LLCR	Low-Level Contact Resistance - Initial		80	mΩ	
Δ LLCR	Low-Level Contact Resistance - Change		10	mΩ	
ESDV	ESD Performance	2 k		V	See Section 3.4.

5.2.5. Current and Voltage Rating Requirements

Table 5-7 lists the contact current rating requirements for PCI Express x1 mated board and cable connectors.

Table 5-7: x1 Current and Voltage Rating Requirements

Symbol	Parameter	Rating	Units	Notes
I_{max}	Contact Current Rating	1.5	A	1
V	Operating Voltage Rating	30	V	

Note:

1. 30 °C maximum temperature rise and 55 °C maximum ambient per ANSI/EIA-364-70.

5.2.6. Mechanical Requirements

Table 5-8 lists the mechanical performance requirements for PCI Express Board-Side connectors.

Table 5-8: x1 Connector Physical and Mechanical Performance Requirements

Symbol	Parameter	Min	Max	Units	Conditions/Comments
F_i	Insertion Force		30	N	Rate = 25 ±6 mm per minute
T_w	Withdrawal Force	5	40	N	Rate = 25 ±6 mm per minute
F_{ls}	Side Load Capability		75	N	
F_{ll}	Longitudinal Load Capability		100	N	
F_{rc}	Housing Contact Retention Force	6.75		N	

5.3. x4 Connector Definition

5.3.1. Pin-out (x4)

Table 5-9 provides the pin assignment for the PCI Express x4 external cable connector. Connector pin assignment is optimized to allow easy assembly of x4 cable configurations while minimizing bow-tie routing on the Board-Side. Receiver and Transmitter pairs are separated by the sideband signals for crosstalk control.

Table 5-9: x4 Connector Pin Assignment

Pin#	Signal	Description	Notes
A1	GND	Ground Reference for PCI Express Transmitter Lanes	
A2	PETp0	Differential PCI Express Transmitter Lane 0	4
A3	PETn0		
A4	GND	Ground Reference for PCI Express Transmitter Lanes	
A5	PETp1	Differential PCI Express Transmitter Lane 1	4
A6	PETn1		
A7	GND	Ground Reference for PCI Express Transmitter Lanes	
A8	PETp2	Differential PCI Express Transmitter Lane 2	4
A9	PETn2		
A10	GND	Ground Reference for PCI Express Transmitter Lanes	
A11	PETp3	Differential PCI Express Transmitter Lane 3	4
A12	PETn3		
A13	GND	Ground Reference for PCI Express Transmitter Lanes	
A14	CREFCLKp	Differential 100 MHz Cable Reference Clock	
A15	CREFCLKn		
A16	GND	Ground Reference for Cable Reference Clock	
A17	SB_RTN	Signal Return for Single Ended Sideband Signals	
A18	CPRSNT#	Used for Detection of Whether a Cable is Installed and the Downstream Subsystem is Powered	
A19	CPWRON	Upstream Subsystem's Power Valid Notification	
B1	GND	Ground Reference for PCI Express Receiver Lanes	
B2	PERp0	Differential PCI Express Receiver Lane 0	4
B3	PERn0		

Pin#	Signal	Description	Notes
B4	GND	Ground Reference for PCI Express Receiver Lanes	
B5	PERp1	Differential PCI Express Receiver Lane 1	4
B6	PERn1		
B7	GND	Ground Reference for PCI Express Receiver Lanes	
B8	PERp2	Differential PCI Express Receiver Lane 2	4
B9	PERn2		
B10	GND	Ground Reference for PCI Express Receiver Lanes	
B11	PERp3	Differential PCI Express Receiver Lane 3	4
B12	PERn3		
B13	GND	Ground Reference for PCI Express Receiver Lanes	
B14	PWR	+3.3 V Power (Optional)	1, 3
B15	PWR	+3.3 V Power (Optional)	1, 3
B16	PWR_RTN	Return for +3.3 V Power (Optional)	1, 3
B17	PWR_RTN	Return for +3.3 V Power (Optional)	1, 3
B18	CWAKE#	Power Management Signal for Wakeup Events (Optional)	1, 2
B19	CPERST#	Cable PERST#	

Notes:

1. Optional signals that are not implemented are to be left as no connects on the Board-Side connector.
2. Board-Side support of CWAKE# is optional; although, an allocated wire is mandated for the cable assembly.
3. These signals are provided for active circuitry within the cable's connector assemblies at the ends of the cable and have no conductor within the cable (i.e., these signals do not actually go across the cable).
4. Board-Side pin-out on both sides of the Link is identical. The cable assembly incorporates a null modem for the PCI Express transmit and receive pairs. Polarity Inversion and Lane Reversal shall not be implemented within the cable assembly.

5.3.2. Board-Side Mechanical Drawings

Figure 5-7 shows an isometric view of the PCI Express x4 Board-Side connector.

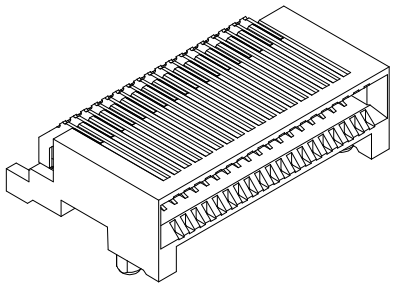


Figure 5-7: Isometric View of x4 Board-Side Connector

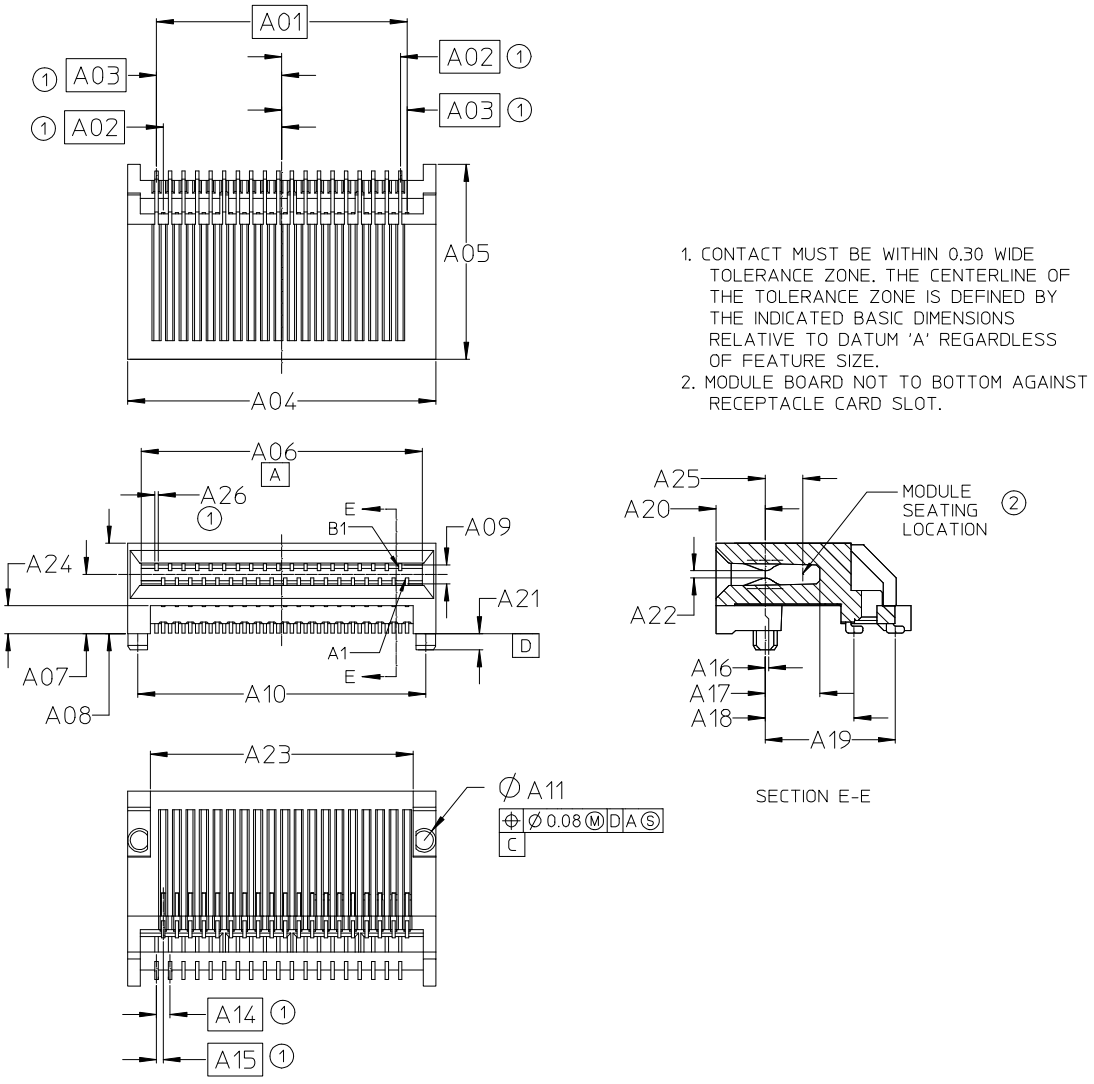


Figure 5-8: x4 Board-Side Connector Form Factor

Table 5-10: x4 Board-Side Connector Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
A01	First to Last	14.80	Basic
A02	CL to First	7.00	Basic
A03	CL to Last	7.40	Basic
A04	Connector Width	18.20	±0.10
A05	OAL Connector Housing	11.50	±0.13
A06	Card Slot Width	16.60	±0.10
A07	PCB to Card Slot CL	3.50	±0.10
A08	OAH Connector Housing	5.35	±0.08
A09	Card Slot Height	1.14	±0.13
A10	Peg to Peg	16.80	Basic
A11	Peg Diameter	1.40	±0.05
A14	Tail Pitch Within Row	0.80	±0.13
A15	Tail Pitch Row to Row	0.40	±0.13
A16	Peg CL to Contact CL	0.00	±0.10
A17	Peg CL to Card Slot	3.22	±0.13
A18	Peg CL to Row A	5.18	±0.10
A19	Peg CL to Row B	7.69	±0.10
A20	Peg CL to Front of Housing	2.90	±0.08
A21	Peg Length	0.95	±0.13
A22	Contact Gap	0.42	±0.13
A23	Leg to Leg	15.53	±0.10
A24	Height Under Connector	1.65	±0.08
A25	Module Seating Location	2.23	Ref
A26	Contact Tolerance Zone	0.30	Max

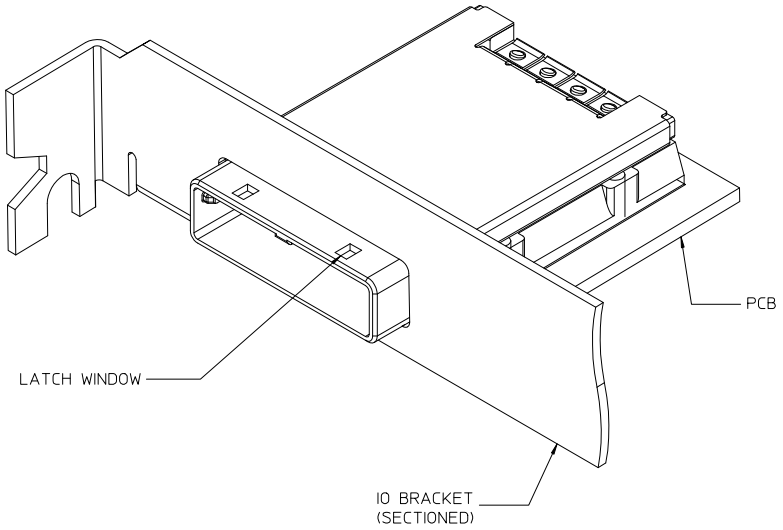


Figure 5-9: x4 EMI Guide Housing Assembly

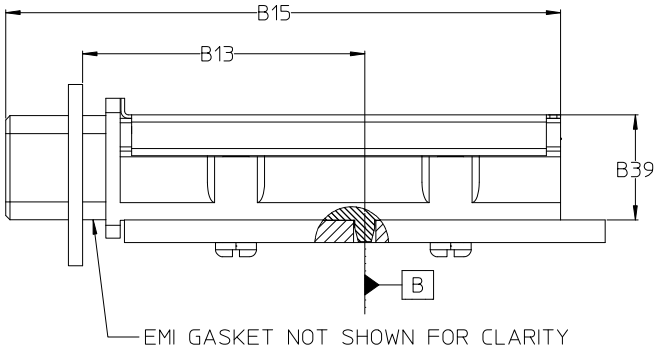


Figure 5-10: x4 Standard (0°) EMI Guide Housing Assembly Side View

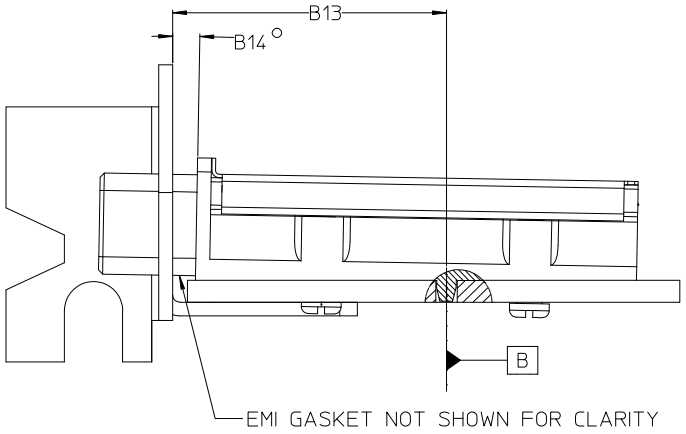


Figure 5-11: x4 PCI Expansion Card (1°) EMI Guide Housing Assembly Side View

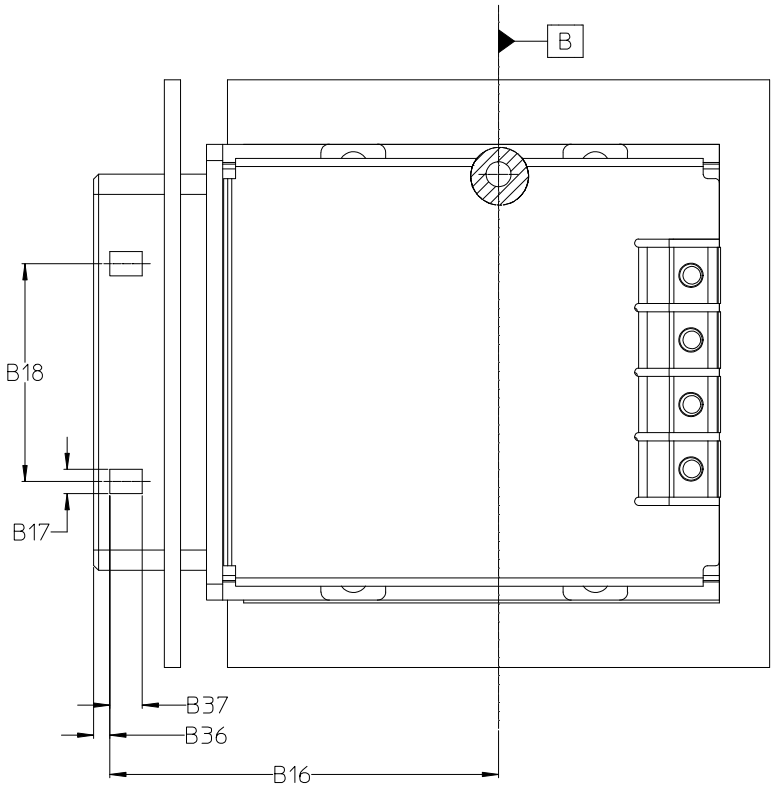


Figure 5-12: x4 EMI Guide Housing Assembly Top View

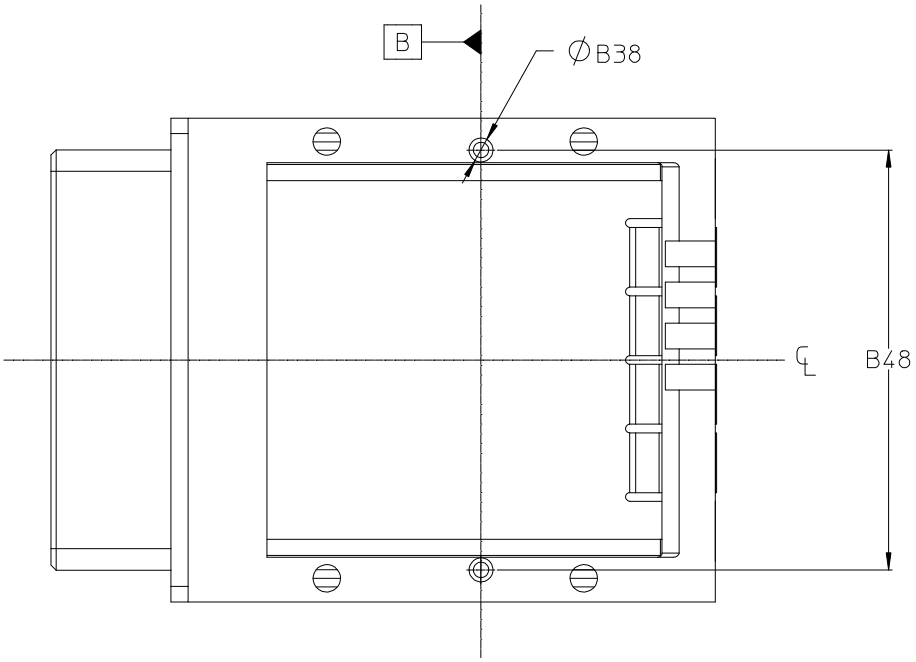


Figure 5-13: x4 EMI Guide Housing Assembly Bottom View

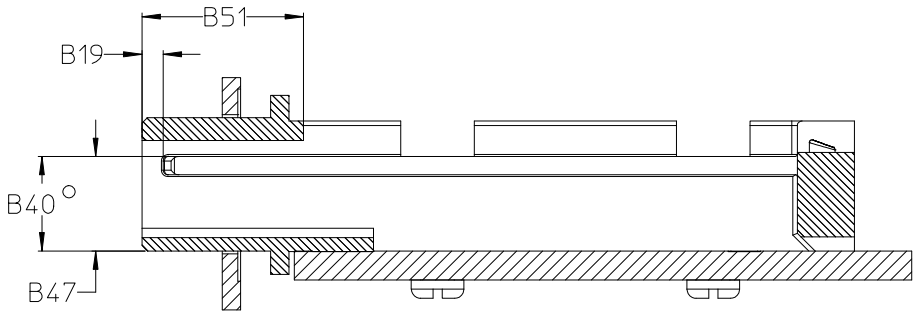


Figure 5-14: x4 (0º) EMI Guide Housing Assembly Section Side View

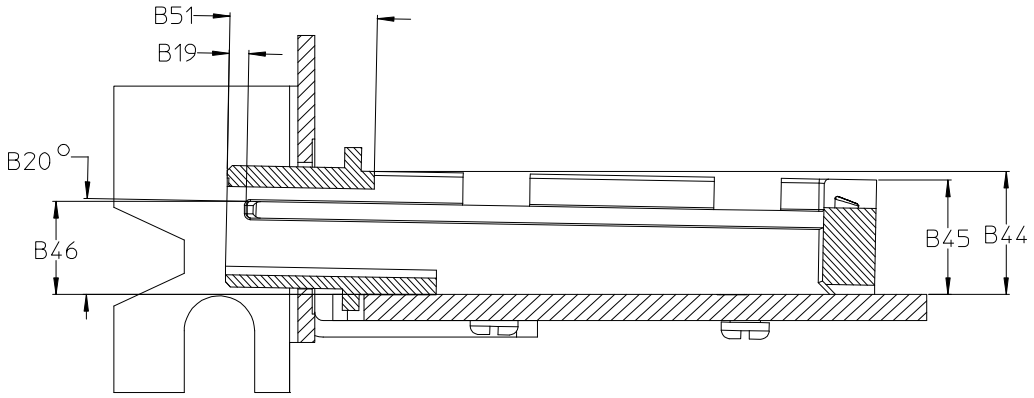


Figure 5-15: x4 (1º) EMI Guide Housing Assembly Section Side View

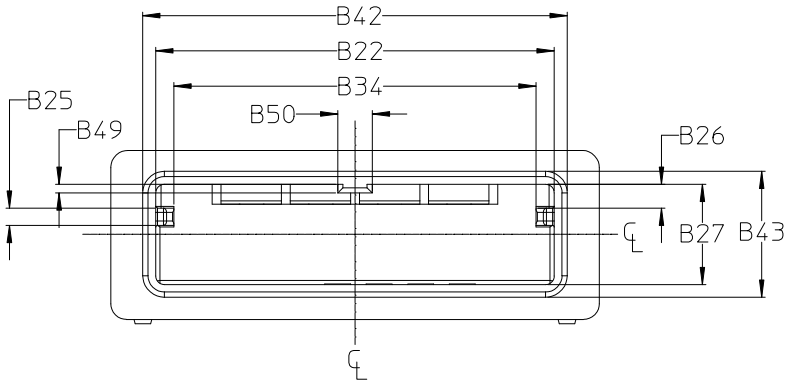


Figure 5-16: x4 EMI Guide Housing Assembly Face View

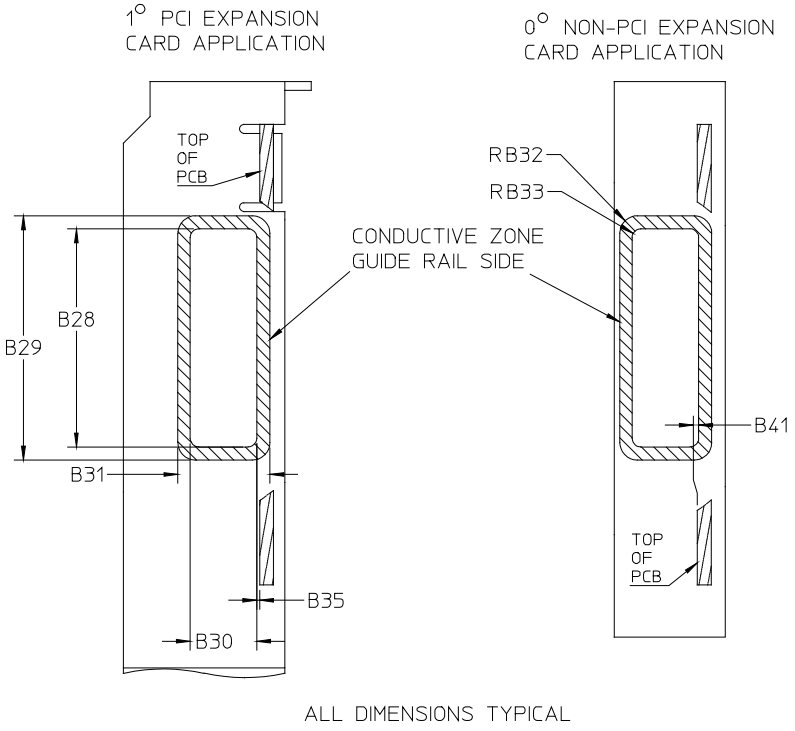


Figure 5-17: x4 EMI Guide Housing Assembly Bracket Window

Table 5-11: x4 EMI Guide Housing Assembly Mechanical Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
B13	Connector Datum to I/O Bracket	19.71	±0.50
B14	Angle	1.00°	±0.5°
B15	Rail Length	38.77	±0.13
B16	Latch Window from Datum B	24.09	±0.05
B17	Latch Window Width	1.50	±0.05
B18	Latch Window to Window Spacing	13.50	±0.05
B19	Rail to Shield Face	1.00	±0.05
B20	Rail Angle	1.00°	Ref
B22	Internal Clearance	23.04	±0.05
B25	Rail Width	1.00	±0.05
B26	Rail to Top Clearance	1.38	±0.05
B27	Internal Clearance	5.84	±0.05
B28	I/O Bracket Cutout Height	25.00	±0.10
B29	Conductive Zone Height	28.00	±0.25
B30	I/O Bracket Cutout Width	7.70	±0.10
B31	Conductive Zone Width	10.50	±0.25

Designator	Description	Dimension (mm)	Tolerance (mm)
B32	Radius	2.00	Max
B33	Radius	1.00	Max
B34	Rail to Rail Inside Spacing	20.94	±0.05
B35	Opening to PCB 1°	0.33	+0.0/-0.13
B36	Latch Window to Cage Forward Edge	1.00	±0.05
B37	Latch Window Length	2.00	±0.05
B38	Locator Peg Diameter	1.46	±0.05
B39	EMI Shield Height	7.38	±0.05
B40	Rail Angle	0.00°	Ref
B41	Opening to PCB 0°	0.20	±0.10
B42	Snout Width	24.54	±0.05
B43	Snout Height	7.29	±0.05
B44	Height at Flange	7.42	±0.05
B45	Height at Rear	6.90	±0.05
B46	Height of Rail 1°	5.61	±0.05
B47	Height of Rail 0°	5.19	±0.05
B48	Locating Pin Spacing	24.52	±0.05
B49	Key Height	0.50	±0.10
B50	Key Width	2.00	±0.10
B51	Key Length	8.79	±0.10

Note:

Although shielding is provided with the connector, in order to meet FCC requirements, gasketing may be required. Gasket mate zones are defined in the above figures. The quality and type of the shielding is application dependent and beyond the scope of this specification.

5.3.3. Recommended Foot Print

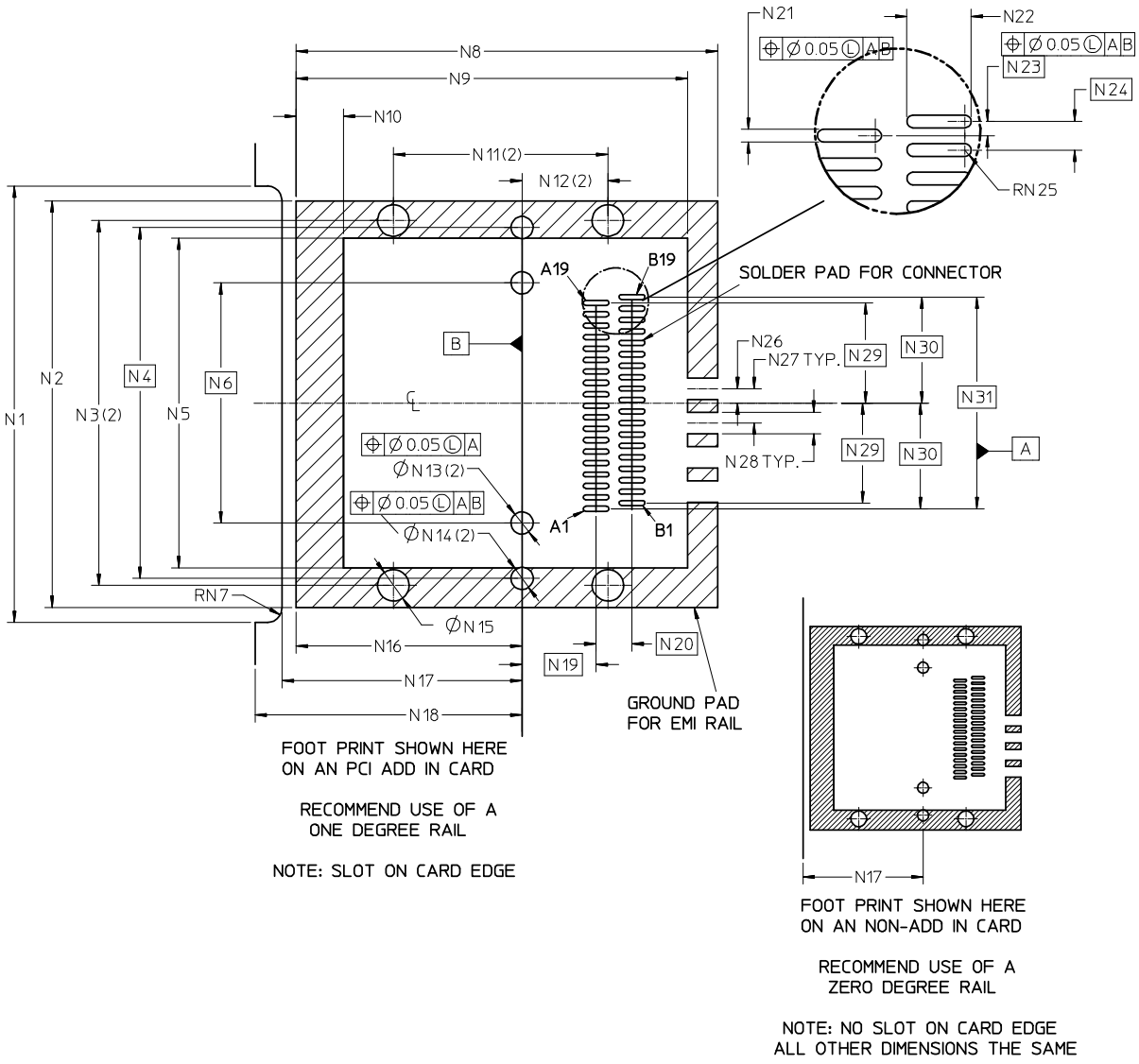


Figure 5-18: x4 Connector and Guide Housing Footprint

Table 5-12: x4 Connector and Guide Housing Footprint Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
N1	Cut Out Width	31.43	Min
N2	Ground Pad Width	28.43	±0.10
N3	Shield Pin Center to Center	25.50	±0.05
N4	Shield Pin Center to Center	24.52	Basic
N5	Window Width	23.04	±0.10
N6	Peg to Peg	16.80	Basic

Designator	Description	Dimension (mm)	Tolerance (mm)
N7	Radius	1.00	±0.05
N8	Ground Pad Length	29.48	±0.10
N9	Card Edge to Ground Pad Edge	27.37	±0.10
N10	Pad Width	3.30	±0.10
N11	Shield Pin to Shield Pin	15.00	±0.05
N12	Connector Pin to Shield Pin	6.00	±0.05
N13	Hole Diameter	1.55	±0.05
N14	Diameter	1.55	±0.05
N15	Diameter	2.20	±0.05
N16	Ground Pad to Card Edge	15.80	±0.10
N17	Connector Datum to Card Edge	16.80	±0.13
N18	Forward Edge of PCB to Datum B	18.67	±0.13
N19	Peg CL to Row A	5.18	Basic
N20	Row A to Row B	2.51	Basic
N21	Pad Width	0.35	±0.03
N22	Pad Length	1.80	±0.03
N23	Tail Pitch Row to Row	0.40	Basic
N24	Tail Pitch Within Row	0.80	Basic
N25	Pad Radius	Full	±0.13
N26	Ground Pad Alley 1 Location from Centerline	1.00	±0.10
N27	Ground Pad Alley Spacing	2.40	±0.10
N28	Ground Pad Alley Width	1.50	±0.10
N29	CL to First	7.00	Basic
N30	CL to Last	7.40	Basic
N31	First to Last	14.80	Basic

5.3.4. Electrical Requirements

Table 5-13 lists the electrical performance requirements for PCI Express x4 mated board and cable connectors.

Table 5-13: x4 Connector Electrical Performance Requirements

Symbol	Parameter	Min	Max	Units	Conditions/Comments
LLCR	Low-Level Contact Resistance - Initial		40	mΩ	
Δ LLCR	Low-Level Contact Resistance - Change		10	mΩ	
ESDV	ESD Performance	2k		V	See Section 3.4.

5.3.5. Current and Voltage Rating Requirements

Table 5-14 lists contact rating requirements for PCI Express x4 mated board and cable connectors.

Table 5-14: x4 Current and Voltage Rating Requirements

Symbol	Parameter	Rating	Units	Notes
I_{max}	Contact Current Rating	0.5	A	1
V	Operating Voltage Rating	30	V	

Notes:

1. 30 °C maximum temperature rise and 55 °C maximum ambient per ANSI/EIA-364-70.

5.3.6. Mechanical Requirements

Table 5-15 lists the mechanical performance requirements for PCI Express x4 cable connectors.

Table 5-15: x4 Connector Physical and Mechanical Performance Requirements

Symbol	Parameter	Min	Max	Units	Conditions/Comments
F_i	Insertion Force		47.5	N	Rate = 25 ±6 mm per minute
T_w	Withdrawal Force	9.5		N	Rate = 25 ±6 mm per minute
F_r	Retention Force		100	N	
F_{ls}	Side Load Capability		75	N	
F_{ll}	Longitudinal Load Capability		100	N	
F_{rc}	Housing Contact Retention Force	2.75		N	
W_c	Contact Wipe	0.4		mm	

Notes:

The guide rail is required to be nickel plated.

5.4. x8 Connector Definition

5.4.1. Pin-out (x8)

Table 5-16 provides the pin assignment for the PCI Express x8 external cable connector. Connector pin assignment is optimized to allow easy assembly of cable configurations while minimizing bow-tie routing on the Board-Side.

Table 5-16: x8 Connector Pin Assignment

Pin#	Signal	Description	Notes
A1	GND	Ground Reference for PCI Express Transmitter Lanes	
A2	PETp0	Differential PCI Express Transmitter Lane 0	5
A3	PETn0		
A4	GND	Ground Reference for PCI Express Transmitter Lanes	
A5	PETp1	Differential PCI Express Transmitter Lane 1	5
A6	PETn1		
A7	GND	Ground Reference for PCI Express Transmitter Lanes	
A8	PETp2	Differential PCI Express Transmitter Lane 2	5
A9	PETn2		

Pin#	Signal	Description	Notes
A10	GND	Ground Reference for PCI Express Transmitter Lanes	
A11	PETp3	Differential PCI Express Transmitter Lane 3	5
A12	PETn3		
A13	GND	Ground Reference for PCI Express Transmitter Lanes	
A14	CREFCLKp	Differential 100 MHz Cable Reference Clock	
A15	CREFCLKn		
A16	GND	Ground Reference for Cable Reference Clock	
A17	RSVD	Reserved	2
A18	RSVD	Reserved	2
A19	SB_RTN	Signal Return for Single Ended Sideband Signals	
A20	CPRSNT#	Used for Detection of Whether a Cable is Installed and the Downstream Subsystem is Powered	
A21	CPWRON	Upstream Subsystem's Power Valid Notification	
A22	GND	Ground Reference for PCI Express Transmitter Lanes	
A23	PETp4	Differential PCI Express Transmitter Lane 4	5, 6
A24	PETn4		
A25	GND	Ground Reference for PCI Express Transmitter Lanes	
A26	PETp5	Differential PCI Express Transmitter Lane 5	5, 6
A27	PETn5		
A28	GND	Ground Reference for PCI Express Transmitter Lanes	
A29	PETp6	Differential PCI Express Transmitter Lane 6	5, 6
A30	PETn6		
A31	GND	Ground Reference for PCI Express Transmitter Lanes	
A32	PETp7	Differential PCI Express Transmitter Lane 7	5, 6
A33	PETn7		
A34	GND	Ground Reference for PCI Express Transmitter Lanes	
B1	GND	Ground Reference for PCI Express Receiver Lanes	
B2	PERp0	Differential PCI Express Receiver Lane 0	5
B3	PERn0		
B4	GND	Ground Reference for PCI Express Receiver Lanes	
B5	PERp1	Differential PCI Express Receiver Lane 1	5
B6	PERn1		
B7	GND	Ground Reference for PCI Express Receiver Lanes	

Pin#	Signal	Description	Notes
B8	PERp2	Differential PCI Express Receiver Lane 2	5
B9	PERn2		
B10	GND	Ground Reference for PCI Express Receiver Lanes	
B11	PERp3	Differential PCI Express Receiver Lane 3	5
B12	PERn3		
B13	GND	Ground Reference for PCI Express Receiver Lanes	
B14	PWR	+3.3 V Power (Optional)	1, 4
B15	PWR	+3.3 V Power (Optional)	1, 4
B16	PWR	+3.3 V Power (Optional)	1, 4
B17	PWR_RTN	Return for +3.3 V Power (Optional)	1, 4
B18	PWR_RTN	Return for +3.3 V Power (Optional)	1, 4
B19	PWR_RTN	Return for +3.3 V Power (Optional)	1,4
B20	CWAKE#	Power Management Signal for Wakeup Events (Optional)	1, 3
B21	CPERST#	Cable PERST#	
B22	GND	Ground Reference for PCI Express Receiver Lanes	
B23	PERp4	Differential PCI Express Receiver Lane 4	5, 6
B24	PERn4		
B25	GND	Ground Reference for PCI Express Receiver Lanes	
B26	PERp5	Differential PCI Express Receiver Lane 5	5, 6
B27	PERn5		
B28	GND	Ground Reference for PCI Express Receiver Lanes	
B29	PERp6	Differential PCI Express Receiver Lane 6	5, 6
B30	PERn6		
B31	GND	Ground Reference for PCI Express Receiver Lanes	
B32	PERp7	Differential PCI Express Receiver Lane 7	5, 6
B33	PERn7		
B34	GND	Ground Reference for PCI Express Receiver Lanes	

Notes:

1. Optional signals that are not implemented are to be left as no connects on the Board-Side connector.
2. Reserved signals shall be left as no connects on the Board-Side connector.
3. Although support of CWAKE# is optional from the Board-Side connector perspective, an allocated wire is mandated for the cable assembly.
4. These signals are provided for active circuitry within the cable's connector assemblies at the ends of the cable and have no conductor within the cable (i.e., these signals do not actually go across the cable).

5. Board-Side pin-out on both sides of the Link is identical. The cable assembly incorporates a null modem for the PCI Express transmit and receive pairs. Polarity Inversion and Lane Reversal shall not be implemented within the cable assembly.
6. PCI Express Lanes 4 through 7 are optional from both a board and cable assembly perspective.

5.4.2. Board-Side Mechanical Drawings

Figure 5-19 shows an isometric view of the PCI Express x8 Board-Side connector.

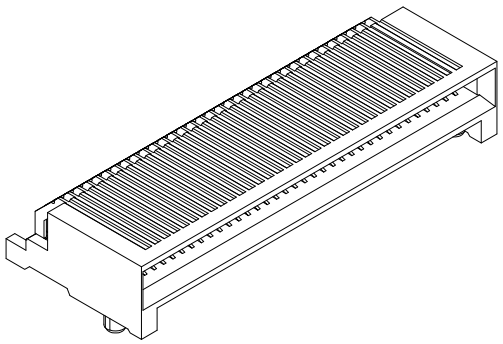


Figure 5-19: Isometric View of x8 Board-Side Connector

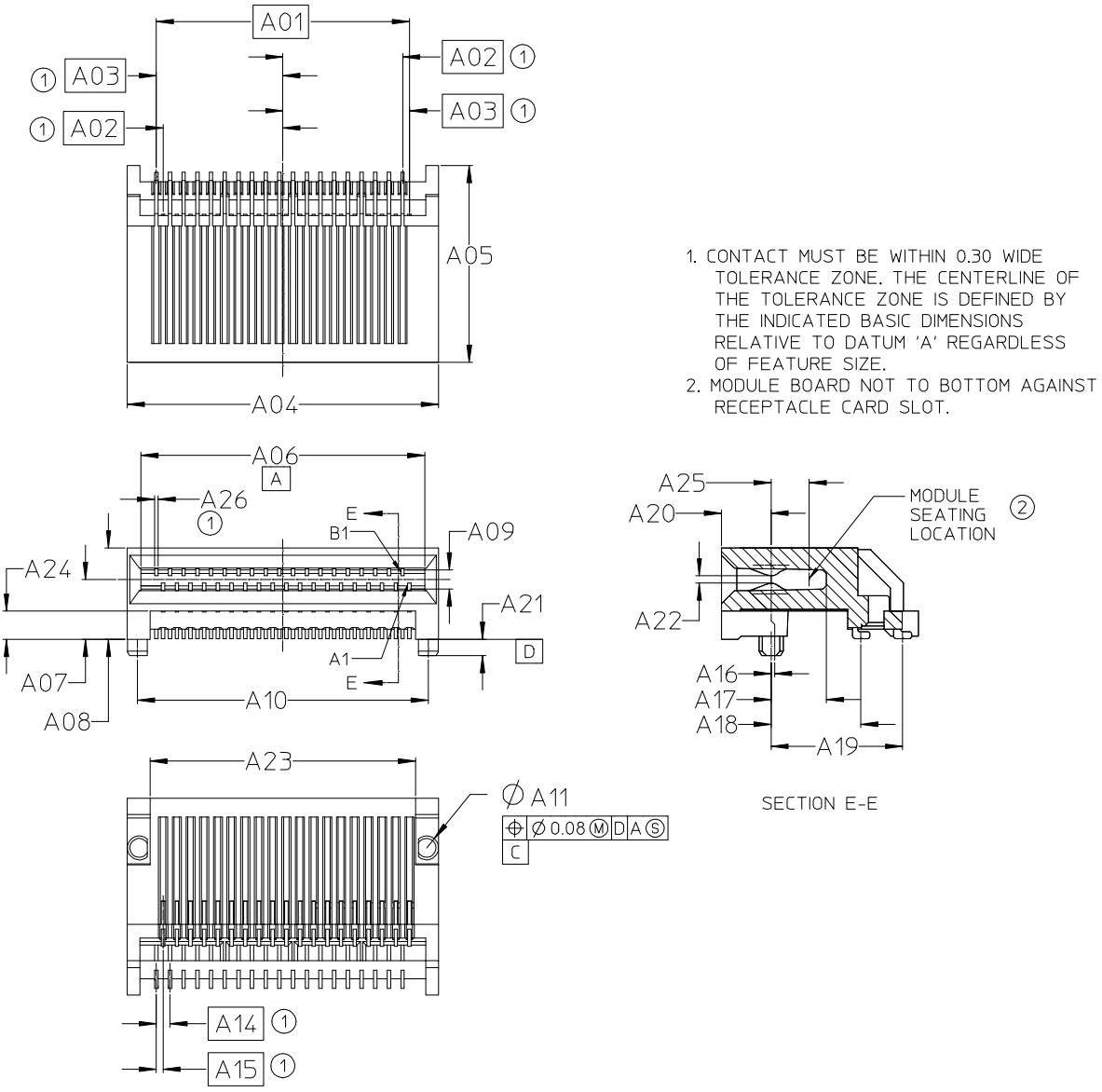


Figure 5-20: x8 Board-Side Connector Form Factor

Table 5-17: x8 Board-Side Connector Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
A01	First to Last	26.80	Basic
A02	CL to First	13.00	Basic
A03	CL to Last	13.40	Basic
A04	Connector Width	30.20	±0.10
A05	OAL Connector Housing	11.50	±0.13
A06	Card Slot Width	28.60	±0.10
A07	PCB to Card Slot CL	3.50	±0.10

Designator	Description	Dimension (mm)	Tolerance (mm)
A08	OAH Connector Housing	5.35	±0.08
A09	Card Slot Height	1.14	±0.13
A10	Peg to Peg	28.80	Basic
A11	Peg Diameter	1.40	±0.05
A14	Tail Pitch Within Row	0.80	±0.13
A15	Tail Pitch Row to Row	0.40	±0.13
A16	Peg CL to Contact CL	0.00	±0.10
A17	Peg CL to Card Slot	3.22	±0.13
A18	Peg CL to Row A	5.18	±0.10
A19	Peg CL to Row B	7.69	±0.10
A20	Peg CL to Front of Housing	2.90	±0.08
A21	Peg Length	0.95	±0.13
A22	Contact Gap	0.42	±0.13
A23	Leg to Leg	27.53	±0.10
A24	Height Under Connector	1.65	±0.08
A25	Module Seating Location	2.23	Ref
A26	Contact Tolerance Zone	0.30	Max

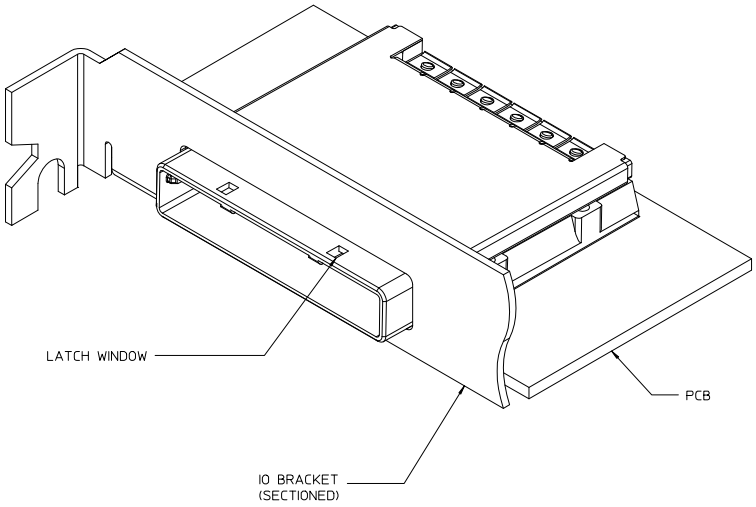


Figure 5-21: x8 EMI Guide Housing Assembly

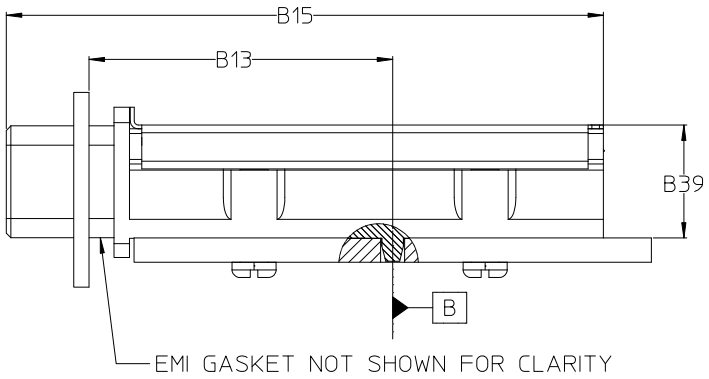


Figure 5-22: x8 Standard (0°) EMI Guide Housing Assembly Side View

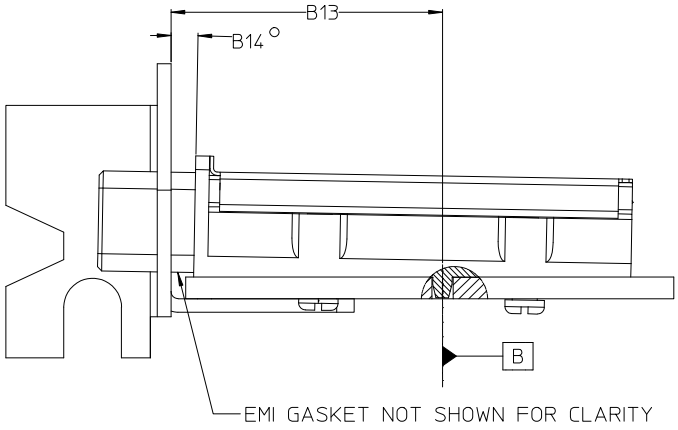


Figure 5-23: x8 Expansion Card (1°) EMI Guide Housing Assembly Side View

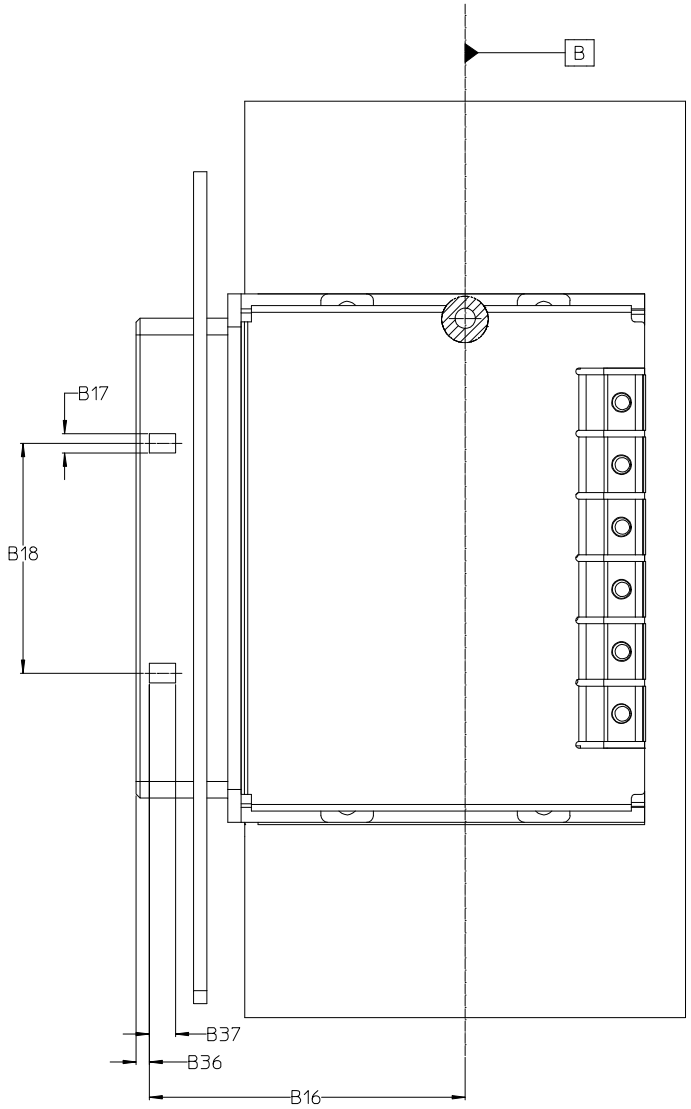


Figure 5-24: x8 EMI Guide Housing Assembly Top View

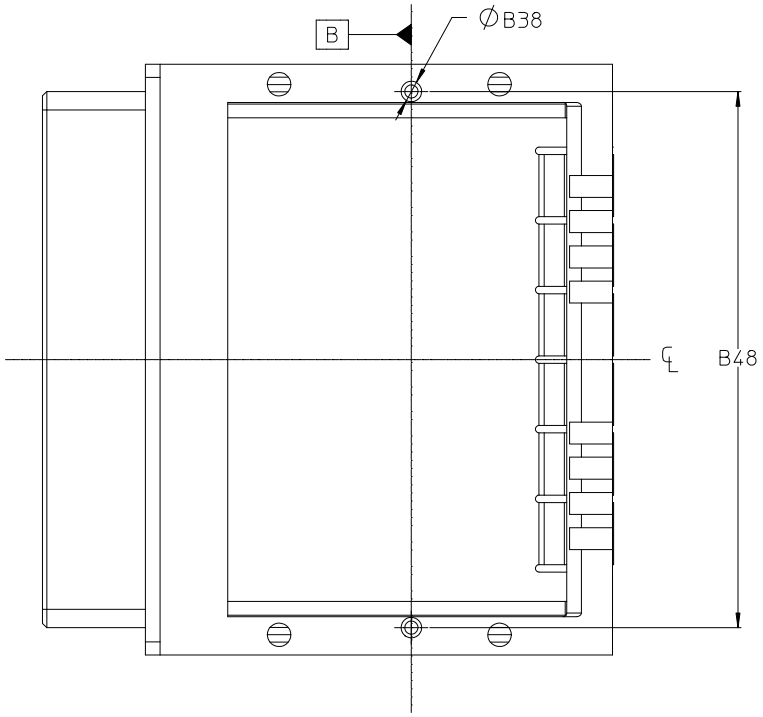


Figure 5-25: x8 EMI Guide Housing Assembly Bottom View

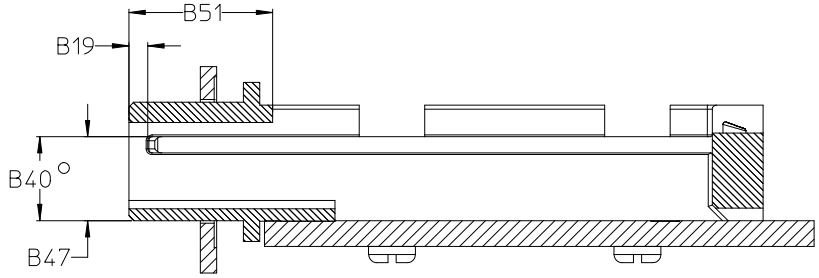


Figure 5-26: x8 (0º) EMI Guide Housing Assembly Section Side View

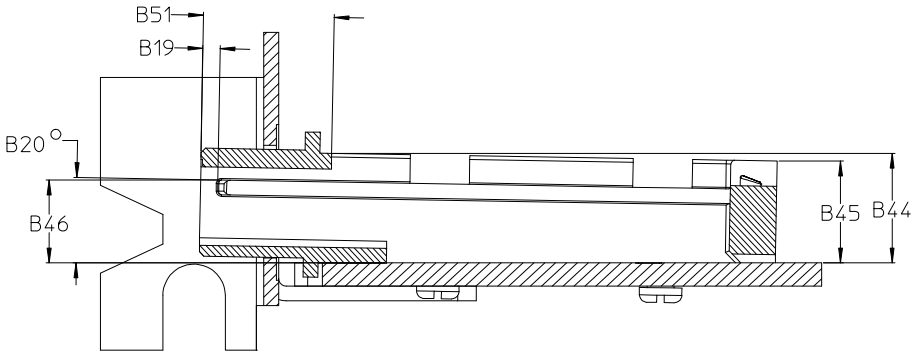


Figure 5-27: x8 (1º) EMI Guide Housing Assembly Section Side View

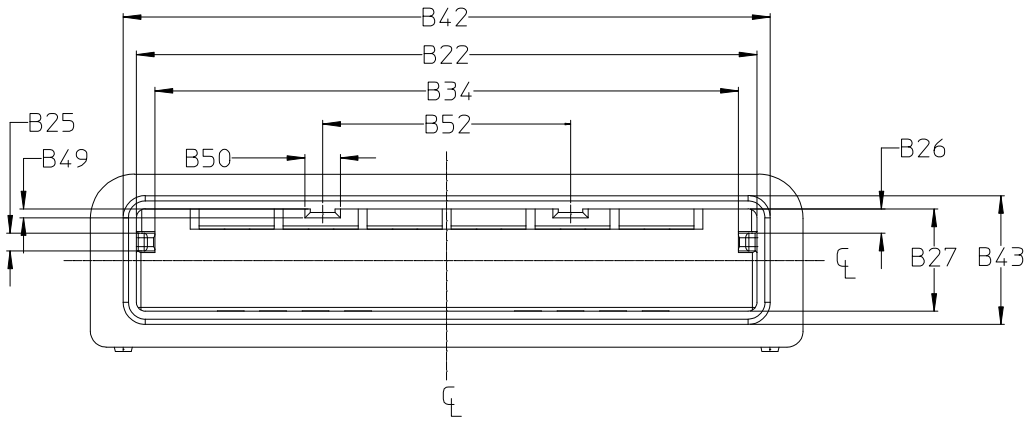


Figure 5-28: x8 EMI Guide Housing Assembly Face View

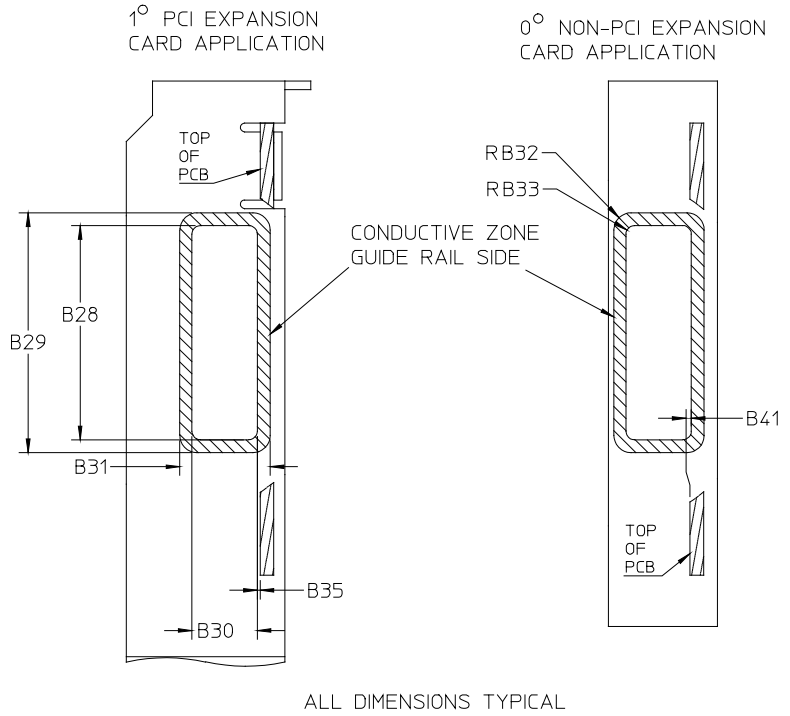


Figure 5-29: x8 EMI Guide Housing Assembly Bracket Window

Table 5-18: x8 EMI Guide Housing Assembly Mechanical Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
B13	Connector Datum to I/O Bracket	19.71	±0.50
B14	Angle	1.00°	±0.5°
B15	Rail Length	38.77	±0.13
B16	Latch Window from Datum B	24.09	±0.05
B17	Latch Window Width	1.50	±0.05
B18	Latch Window to Window Spacing	17.50	±0.05
B19	Rail to Shield Face	1.00	±0.05
B20	Rail Angle	1.00°	Ref
B22	Internal Clearance	35.04	±0.05
B25	Rail Width	1.00	±0.05
B26	Rail to Top Clearance	1.38	±0.05
B27	Internal Clearance	5.84	±0.05
B28	I/O Bracket Cutout Height	37.00	±0.10
B29	Conductive Zone Height	40.00	±0.25
B30	I/O Bracket Cutout Width	10.50	±0.25
B31	Conductive Zone Width	7.70	±0.10
B32	Radius	2.00	Max
B33	Radius	1.00	Max
B34	Rail to Rail Inside Spacing	32.94	±0.05
B35	Opening to PCB 1°	0.33	+0.0/-0.13
B36	Latch Window to Cage Forward Edge	1.00	±0.05
B37	Latch Window Length	2.00	±0.05
B38	Locator Peg Diameter	1.46	±0.05
B39	EMI Shield Height	7.38	±0.05
B40	Rail Angle	0.00°	±0.5°
B41	Opening to PCB 0°	0.20	±0.01
B42	Snout Width	36.54	±0.05
B43	Snout Height	7.29	±0.05
B44	Height at Flange	7.42	±0.05
B45	Height at Rear	6.90	±0.05
B46	Height of Rail 1°	5.61	±0.05
B47	Height of Rail 0°	5.19	±0.05
B48	Locating Pin Spacing	36.52	±0.05

Designator	Description	Dimension (mm)	Tolerance (mm)
B49	Key Height	0.50	±0.10
B50	Key Width	2.00	±0.10
B51	Key Length	8.79	±0.10
B52	Key Location	14.00	±0.10

Note:

Although shielding is provided with the connector, in order to meet FCC requirements, gasketing may be required. Gasket mate zones are defined in the above figures. The quality and type of the shielding is application dependent and beyond the scope of this specification.

5.4.3. Recommended Footprint

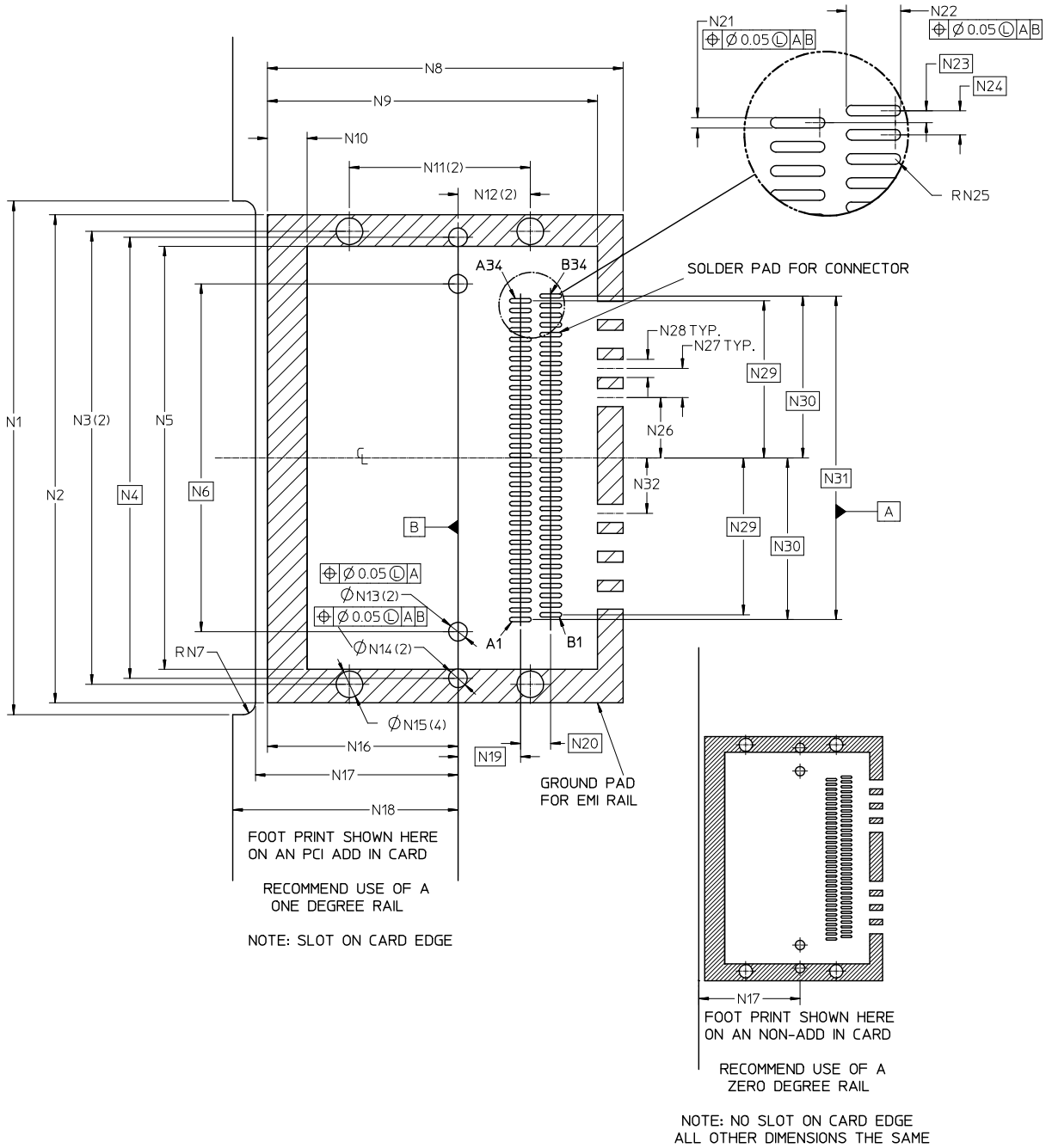


Figure 5-30: x8 Connector and Guide Housing Footprint

Table 5-19: x8 Connector and Guide Housing Footprint Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
N1	Cut Out Width	43.43	Min
N2	Ground Pad Width	40.43	±0.1
N3	Shield Pin Center to Center	37.50	±0.05
N4	Shield Pin Center to Center	36.52	Basic
N5	Window Width	35.04	±0.1
N6	Peg to Peg	28.80	Basic
N7	Radius	1.00	±0.05
N8	Ground Pad Length	29.48	±0.10
N9	Card Edge to Ground Pad Edge	27.37	±0.10
N10	Pad Width	3.30	±0.10
N11	Shield Pin to Shield Pin	15.00	±0.05
N12	Connector Pin to Shield Pin	6.00	±0.05
N13	Hole Diameter	1.55	±0.05
N14	Diameter	1.55	±0.05
N15	Diameter	2.20	±0.05
N16	Ground Pad to Card Edge	15.80	±0.10
N17	Connector Datum to Card Edge	16.80	±0.13
N18	Forward Edge of PCB to Datum B	18.67	±0.13
N19	Peg CL to Row A	5.18	Basic
N20	Row A to Row B	2.51	Basic
N21	Pad Width	0.35	±0.03
N22	Pad Length	1.80	±0.03
N23	Tail Pitch Row to Row	0.40	Basic
N24	Tail Pitch Within Row	0.80	Basic
N25	Pad Radius	Full	±0.13
N26	Ground Pad Alley 1 Location from Centerline	5.00	±0.1
N27	Ground Pad Alley Spacing	2.40	±0.1
N28	Ground Pad Alley Width	1.50	±0.1
N29	CL to First	13.00	Basic
N30	CL to Last	13.40	Basic
N31	First to Last	26.80	Basic
N32	Ground Pad Alley 1 Group 2 from Centerline	4.60	±0.05

5.4.4. Electrical Requirements

Table 5-20 lists the electrical performance requirements for PCI Express x8 mated board and cable connectors.

Table 5-20: x8 Connector Electrical Requirements

Symbol	Parameter	Min	Max	Units	Conditions/Comments
LLCR	Low-Level Contact Resistance - Initial		40	mΩ	
Δ LLCR	Low-Level Contact Resistance - Change		10	mΩ	
ESDV	ESD Performance	2k		V	See Section 3.4

5.4.5. Current and Voltage Rating Requirements

Table 5-21 lists contact rating requirements for PCI Express x8 mated board and cable connectors.

Table 5-21: x8 Current and Voltage Rating Requirements

Symbol	Parameter	Rating	Units	Notes
I_{max}	Contact Current Rating	0.5	A	1
V	Operating Voltage Rating	30	V	

Notes:

1. 30 °C maximum temperature rise and 55 °C maximum ambient per ANSI/EIA-364-70.

5.4.6. Mechanical Requirements

Table 5-22 lists the mechanical performance requirements for PCI Express x8 cable connectors.

Table 5-22: x8 Connector Physical and Mechanical Requirements

Symbol	Parameter	Min	Max	Units	Conditions/Comments
F_i	Insertion Force		85	N	Rate = 25 ±6 mm per minute
T_w	Withdrawal Force	17		N	Rate = 25 ±6 mm per minute
F_r	Retention Force		100	N	
F_{ls}	Side Load Capability		75	N	
F_{ll}	Longitudinal Load Capability		100	N	
F_{rc}	Housing Contact Retention Force	2.75		N	
W_c	Contact Wipe	0.4		mm	

Notes:

The guide rail is required to be nickel plated.

5.5. x16 Connector Definition

5.5.1. Pin-out (x16)

Table 5-23 provides the pin assignment for the PCI Express x16 external cable connector. Connector pin assignment is optimized to allow easy assembly of x16 cable configurations while minimizing bow-tie routing on the Board-Side.

Pin assignment of the Upstream and Downstream Subsystem are different for the x16 implementation. Only the sideband signals are affected where for instance a signal assigned to pin A17 (SB_RTN) at the Upstream Subsystem is to be connected to C17 within the Downstream Subsystem. This requirement is identified, in Table 5-23, by superseding the signal name with a "u" or "d" to identify Upstream versus Downstream Subsystem.

Table 5-23: x16 Connector Pin Assignment

Pin#	Signal	Description	Notes
A1	GND	Ground Reference for PCI Express Receiver Lanes	
A2	PERp1	Differential PCI Express Receiver Lane 1	5
A3	PERn1		
A4	GND	Ground Reference for PCI Express Receiver Lanes	

Pin#	Signal	Description	Notes
A5	PERp3	Differential PCI Express Receiver Lane 3	5
A6	PERn3		
A7	GND	Ground Reference for PCI Express Receiver Lanes	
A8	PERp5	Differential PCI Express Receiver Lane 5	5
A9	PERn5		
A10	GND	Ground Reference for PCI Express Receiver Lanes	
A11	PERp7	Differential PCI Express Receiver Lane 7	5
A12	PERn7		
A13	GND	Ground Reference for PCI Express Receiver Lanes	
A14	PWR	+3.3 V Power (Optional)	1, 4
A15	PWR	+3.3 V Power (Optional)	1, 4
A16	PWR	+3.3 V Power (Optional)	1, 4
A17	uSB_RTN	Signal Return for Single Ended Sideband Signals (GND)	6, 7
A18	GND	Ground Reference for Cable Reference Clock	
A19	uREFCLKp	Differential 100 MHz Cable Reference Clock at Upstream Subsystem	6, 7
A20	uREFCLKn		
A21	GND	Ground Reference for PCI Express Receiver Lanes	
A22	PERp9	Differential PCI Express Receiver Lane 9	5
A23	PERn9		
A24	GND	Ground Reference for PCI Express Receiver Lanes	
A25	PERp11	Differential PCI Express Receiver Lane 11	5
A26	PERn11		
A27	GND	Ground Reference for PCI Express Receiver Lanes	
A28	PERp13	Differential PCI Express Receiver Lane 13	5
A29	PERn13		
A30	GND	Ground Reference for PCI Express Receiver Lanes	
A31	PERp15	Differential PCI Express Receiver Lane 15	5
A32	PERn15		
A33	GND	Ground Reference for PCI Express Receiver Lanes	
A34	RSVD	Reserved	2
B1	GND	Ground Reference for PCI Express Receiver Lanes	
B2	PERp0	Differential PCI Express Receiver Lane 0	5
B3	PERn0		
B4	GND	Ground Reference for PCI Express Receiver Lanes	

Pin#	Signal	Description	Notes
B5	PERp2	Differential PCI Express Receiver Lane 2	5
B6	PERn2		
B7	GND	Ground Reference for PCI Express Receiver Lanes	
B8	PERp4	Differential PCI Express Receiver Lane 4	5
B9	PERn4		
B10	GND	Ground Reference for PCI Express Receiver Lanes	
B11	PERp6	Differential PCI Express Receiver Lane 6	5
B12	PERn6		
B13	GND	Ground Reference for PCI Express Receiver Lanes	
B14	PWR_RTN	Return for +3.3 V Power (Optional)	1, 4
B15	PWR_RTN	Return for +3.3 V Power (Optional)	1, 4
B16	PWR_RTN	Return for +3.3 V Power (Optional)	1, 4
B17	uPWRON	Power Valid Notification at Upstream Subsystem	6, 7
B18	uWAKE#	Power Management Signal for Wakeup Events (Optional)	1, 3, 6, 7
B19	uPRSNT#	Used for Detection if a Cable is Installed	6, 7
B20	uPERST#	Cable PERST# at Upstream Subsystem	6, 7
B21	GND	Ground Reference for PCI Express Receiver Lanes	
B22	PERp8	Differential PCI Express Receiver Lane 8	5
B23	PERn8		
B24	GND	Ground Reference for PCI Express Receiver Lanes	
B25	PERp10	Differential PCI Express Receiver Lane 10	5
B26	PERn10		
B27	GND	Ground Reference for PCI Express Receiver Lanes	
B28	PERp12	Differential PCI Express Receiver Lane 12	5
B29	PERn12		
B30	GND	Ground Reference for PCI Express Receiver Lanes	
B31	PERp14	Differential PCI Express Receiver Lane 14	5
B32	PERn14		
B33	GND	Ground Reference for PCI Express Receiver Lanes	
B34	RSVD	Reserved	2
C1	GND	Ground Reference for PCI Express Transmitter Lanes	
C2	PETp1	Differential PCI Express Transmitter Lane 1	5
C3	PETn1		
C4	GND	Ground Reference for PCI Express Transmitter Lanes	

Pin#	Signal	Description	Notes
C5	PETp3	Differential PCI Express Transmitter Lane 3	5
C6	PETn3		
C7	GND	Ground Reference for PCI Express Transmitter Lanes	
C8	PETp5	Differential PCI Express Transmitter Lane 5	5
C9	PETn5		
C10	GND	Ground Reference for PCI Express Transmitter Lanes	
C11	PETp7	Differential PCI Express Transmitter Lane 7	5
C12	PETn7		
C13	GND	Ground Reference for PCI Express Transmitter Lanes	
C14	PWR	+3.3 V Power (Optional)	1, 4
C15	PWR	+3.3 V Power (Optional)	1, 4
C16	PWR	+3.3 V Power (Optional)	1, 4
C17	dSB_RTN	Signal Return for Single-Ended Signals at Downstream Subsystem	6, 7
C18	GND	Ground Reference for Cable Reference Clock	
C19	dREFCLKp	Differential 100 MHz Cable Reference Clock at Downstream Subsystem	6, 7
C20	dREFCLKn		
C21	GND	Ground Reference for PCI Express Transmitter Lanes	
C22	PETp9	Differential PCI Express Transmitter Lane 9	5
C23	PETn9		
C24	GND	Ground Reference for PCI Express Transmitter Lanes	
C25	PETp11	Differential PCI Express Transmitter Lane 11	5
C26	PETn11		
C27	GND	Ground Reference for PCI Express Transmitter Lanes	
C28	PETp13	Differential PCI Express Transmitter Lane 13	5
C29	PETn13		
C30	GND	Ground Reference for PCI Express Transmitter Lanes	
C31	PETp15	Differential PCI Express Transmitter Lane 15	5
C32	PETn15		
C33	GND	Ground Reference for PCI Express Transmitter Lanes	
C34	RSVD	Reserved	2
D1	GND	Ground Reference for PCI Express Transmitter Lanes	
D2	PETp0	Differential PCI Express Transmitter Lane 0	5
D3	PETn0		
D4	GND	Ground Reference for PCI Express Transmitter Lanes	

Pin#	Signal	Description	Notes
D5	PETp2	Differential PCI Express Transmitter Lane 2	5
D6	PETn2		
D7	GND	Ground Reference for PCI Express Transmitter Lanes	
D8	PETp4	Differential PCI Express Transmitter Lane 4	5
D9	PETn4		
D10	GND	Ground Reference for PCI Express Transmitter Lanes	
D11	PETp6	Differential PCI Express Transmitter Lane 6	5
D12	PETn6		
D13	GND	Ground Reference for PCI Express Transmitter Lanes	
D14	PWR_RTN	Return for +3.3 V Power (Optional)	1, 4
D15	PWR_RTN	Return for +3.3 V Power (Optional)	1, 4
D16	PWR_RTN	Return for +3.3 V Power (Optional)	1,4
D17	dPWRON	Power Valid Notification	6, 7
D18	dWAKE#	Power Management for Wakeup Events at Downstream Subsystem	1, 3, 6, 7
D19	dPRSNT#	Used for Detection if a Cable is Installed	6, 7
D20	dPERST#	Cable PERST# at Downstream Subsystem	6, 7
D21	GND	Ground Reference for PCI Express Transmitter Lanes	
D22	PETp8	Differential PCI Express Transmitter Lane 8	5
D23	PETn8		
D24	GND	Ground Reference for PCI Express Transmitter Lanes	
D25	PETp10	Differential PCI Express Transmitter Lane 10	5
D26	PETn10		
D27	GND	Ground Reference for PCI Express Transmitter Lanes	
D28	PETp12	Differential PCI Express Transmitter Lane 12	5
D29	PETn12		
D30	GND	Ground Reference for PCI Express Transmitter Lanes	
D31	PETp14	Differential PCI Express Transmitter Lane 14	5
D32	PETn14		
D33	GND	Ground Reference for PCI Express Transmitter Lanes	
D34	RSVD	Reserved	2

Notes:

1. Optional signals that are not implemented are to be left as no connects on the Board-Side connector.
2. Reserved signals shall be left as no connects on the Board-Side connector.
3. Although support of CWAKE# is optional from the Board-Side connector perspective, an allocated wire is mandated for the cable assembly.

4. These signals are provided for active circuitry within the cable's connector assemblies at the ends of the cable and have no conductor within the cable (i.e., these signals do not actually go across the cable).
5. Board-Side pin-out on both sides of the Link is *not* identical. Sideband signals have been assigned to different pin numbers to facilitate cable assembly manufacturing, see Notes 6 and 7 below. The cable assembly incorporates a null modem for the PCI Express transmit and receive pairs. Polarity Inversion and Lane Reversal shall not be implemented within the cable assembly.
6. Pins A17, A19, A20, B17, B18, B19, and B20 connect to the appropriate sideband signal within the Upstream Subsystem. These connector pins shall be terminated to ground within the Downstream Subsystem.
7. Pins C17, C19, C20, D17, D18, D19, and D20 connect to the appropriate sideband signal within the Downstream Subsystem. These connector pins shall be terminated to ground within the Upstream Subsystem.

5.5.2. Board-Side Mechanical Drawings

Figure 5-31 shows an isometric view of the PCI Express x16 connector.

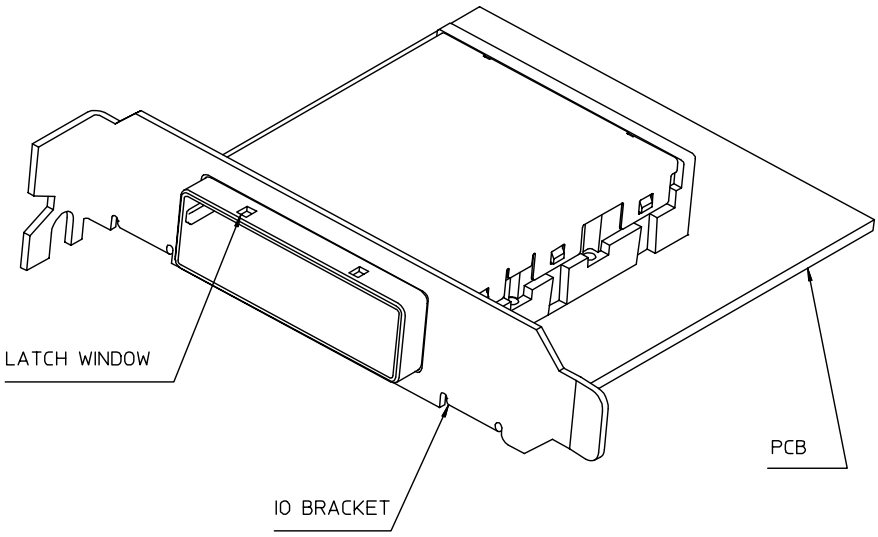


Figure 5-31: Isometric View of x16 Connector Assembly

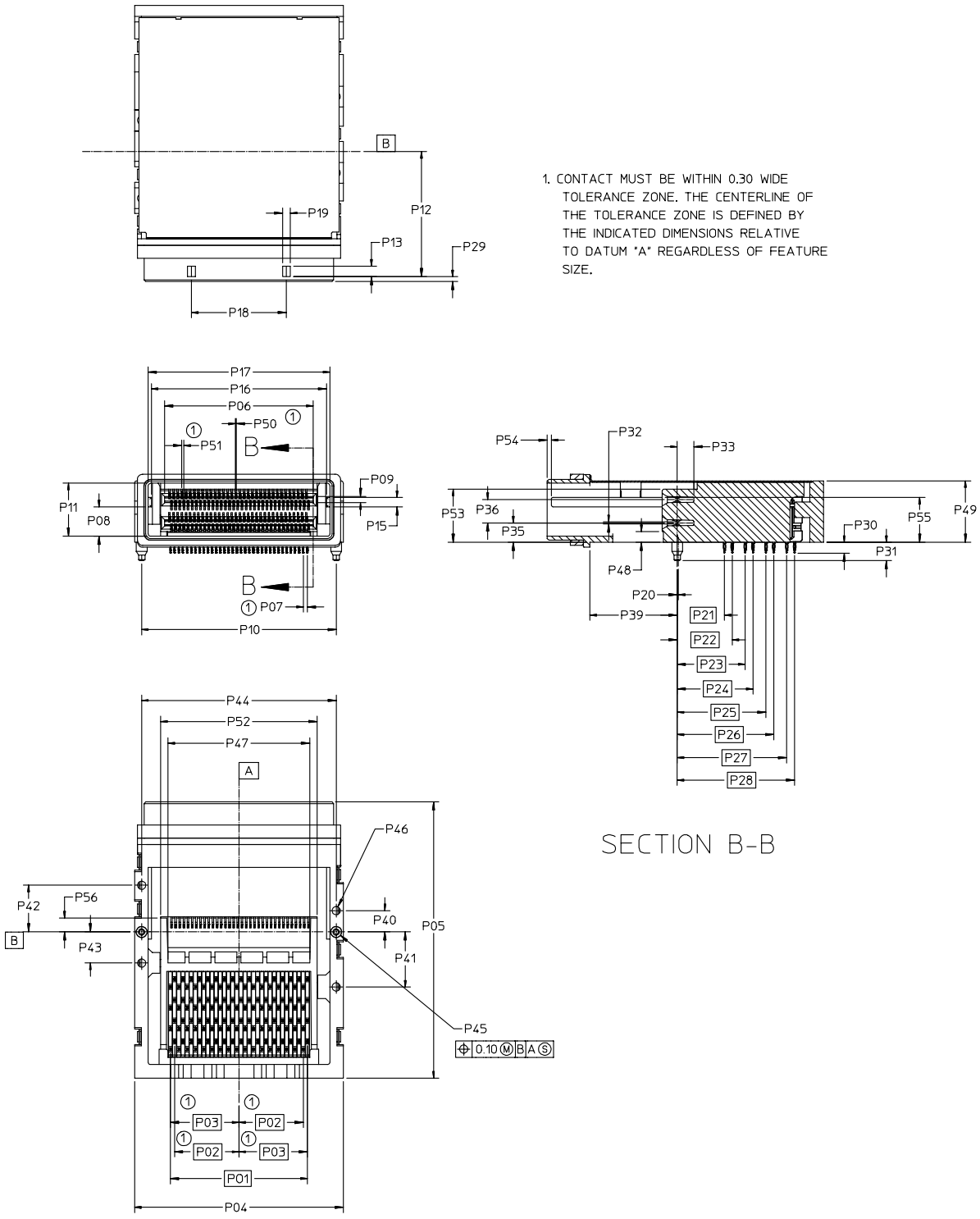


Figure 5-32: x16 Board-Side Connector Form Factor

Table 5-24: x16 Board-Side Connector Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
P01	First to Last	26.40	Basic
P02	CL to First	12.40	Basic
P03	CL to Last	13.20	Basic
P04	Connector Width	40.25	±0.25
P05	OAL Connector Housing	53.25	±0.25
P06	Card Slot Width	28.60	±0.10
P07	Tail Pitch	0.80	Basic
P08	Housing Guide Rib Location	5.67	±0.08
P09	Card Slot Height	1.14	±0.13
P10	Peg to Peg	37.50	±0.10
P11	Connector Opening	10.20	±0.05
P12	Opening to Latch Hole	24.09	±0.05
P13	Latch Hole Depth	2.00	±0.13
P15	Guide Rib Thickness	1.80	±0.13
P16	Housing Opening Rib to Rib	33.75	±0.05
P17	Housing Opening	35.04	±0.05
P18	Latch Hole CL to CL	17.50	±0.05
P19	Latch Hole Width	1.50	±0.13
P20	Peg CL to Contact CL	0.00	±0.10
P21	Peg CL to Row A	9.10	Basic
P22	Peg CL to Row B	10.60	Basic
P23	Peg CL to Row C	13.10	Basic
P24	Peg CL to Row D	14.60	Basic
P25	Peg CL to Row E	17.10	Basic
P26	Peg CL to Row F	18.60	Basic
P27	Peg CL to Row G	21.10	Basic
P28	Peg CL to Row H	22.60	Basic
P29	Peg CL to Front of Connector	1.00	±0.05
P30	Contact Tail Length	2.08	±0.13
P31	Peg Length	3.50	±0.13
P32	Contact Gap	0.42	±0.13
P33	Peg CL to Card Slot	3.22	±0.13
P35	PCB to First Card Slot	3.75	±0.10

Designator	Description	Dimension (mm)	Tolerance (mm)
P36	First Card Slot to Second Card Slot	4.50	±0.10
P39	Peg CL to Housing Lip	16.85	±0.13
P40	Peg CL to Right Front Mounting Hole	4.10	±0.13
P41	Peg CL to Right Rear Mounting Hole	10.60	±0.13
P42	Peg CL to Left Front Mounting Hole	9.00	±0.13
P43	Peg CL to Left Rear Mounting Hole	6.00	±0.13
P44	Mounting Hole to Mounting Hole	37.5	±0.05
P45	Peg Diameter	2.08	±0.05
P46	Mounting Hole Diameter	1.78	±0.10
P47	Leg to Leg	27.58	±0.13
P48	PCB to Bottom of Housing	2.08	±0.13
P49	PCB to Cover	11.88	±0.13
P50	Contact Tolerance Zone	0.30	Max
P51	Contact Pitch Row to Row	0.40	±0.13
P52	Receptacle Connector Housing	30.20	±0.10
P53	OAH of Receptacle Connector	10.22	±0.13
P54	Rail to Shield Face	0.84	±0.05
P55	Rail to PCB	8.64	±0.05
P56	Receptacle Face to Pegs	2.66	±0.08

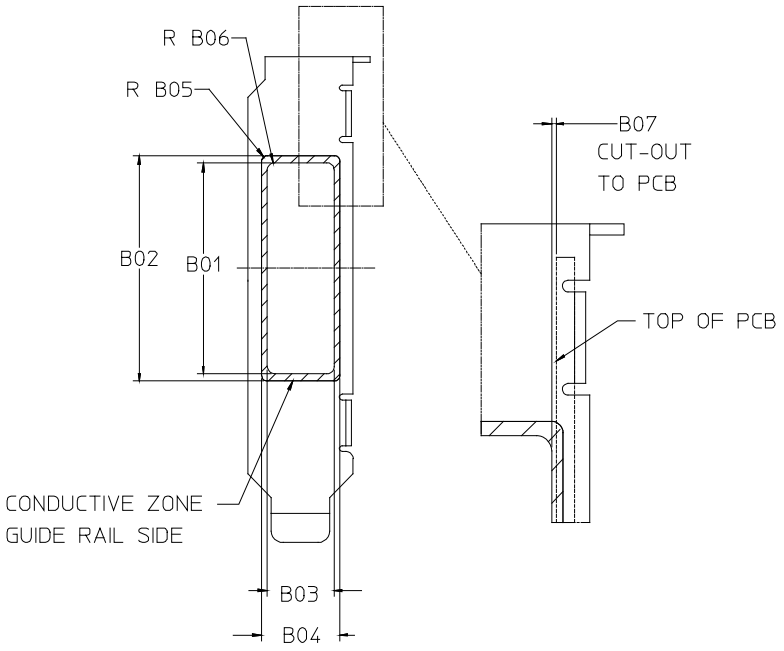


Figure 5-33: x16 Connector Assembly Bracket Window

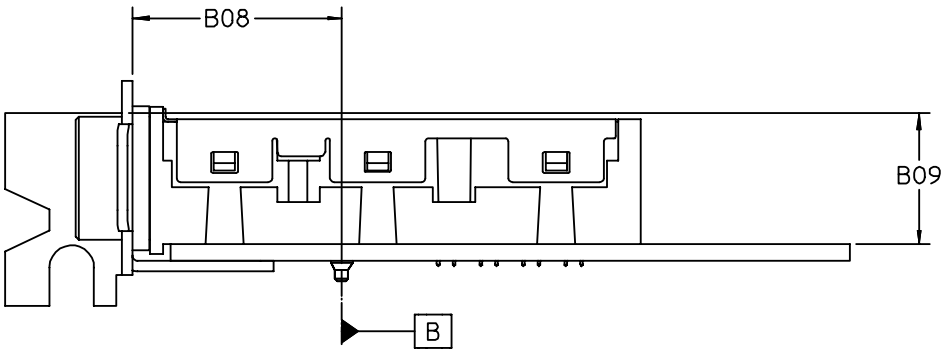


Figure 5-34: x16 Connector Assembly Side View

Table 5-25: x16 Connector Assembly Bracket Window Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
B01	I/O Bracket Cutout Height	37.00	±0.05
B02	Conductive Zone Height	40.00	±0.05
B03	I/O Bracket Cutout Width	12.00	±0.05
B04	Conductive Zone Width	14.90	±0.05
B05	Radius	2.00	±0.05
B06	Radius	1.00	±0.05
B07	Opening to PCB	0.33	±0.05
B08	Connector Datum to I/O Bracket	19.71	±0.50
B09	PCB to Panel Opening	12.33	±0.05

Notes:

Although shielding is provided with the connector, in order to meet FCC requirements, gasketing may be required. Gasket mate zones are defined in the above figures. The quality and type of the shielding is application dependent and beyond the scope of this specification.

5.5.3. Recommended Footprint

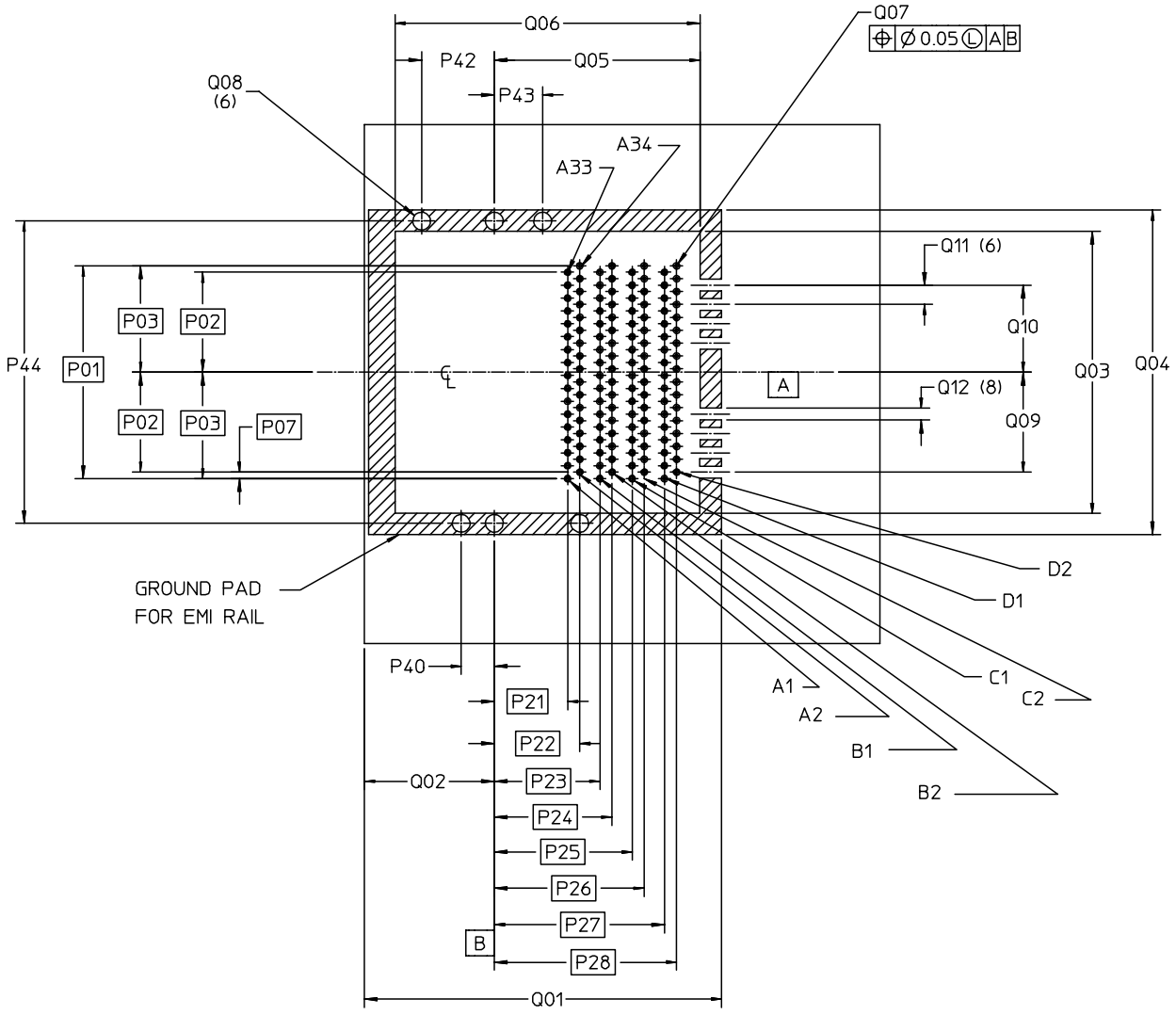


Figure 5-35: x16 Connector Assembly Footprint

Table 5-26: x16 Connector Assembly Footprint Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
P01	First to Last	26.40	Basic
P02	CL to First	12.40	Basic
P03	CL to Last	13.20	Basic
P07	Tail Pitch	0.80	Basic
P21	Peg CL to Row A	9.10	Basic
P22	Peg CL to Row B	10.60	Basic
P23	Peg CL to Row C	13.10	Basic
P24	Peg CL to Row D	14.60	Basic
P25	Peg CL to Row E	17.10	Basic
P26	Peg CL to Row F	18.60	Basic
P27	Peg CL to Row G	21.10	Basic
P28	Peg CL to Row H	22.60	Basic
P40	Peg CL to Right Front Mounting Hole	4.10	±0.13
P42	Peg CL to Left Front Mounting Hole	9.00	±0.13
P43	Peg CL to Left Rear Mounting Hole	6.00	±0.13
P44	Mounting Hole to Mounting Hole	37.50	±0.13
Q01	Ground Plane OAL	44.25	±0.25
Q02	Peg CL to Front of Ground Plane	16.08	±0.25
Q03	Ground Plane Edge to Edge	35.04	±0.25
Q04	Ground Plane OAW	40.25	±0.25
Q05	Peg CL to Back of Ground Plane	25.50	±0.25
Q06	Ground Plane Inside Length	37.80	±0.25
Q07	Hole Diameter	0.46	±0.05
Q08	Mounting Hole	2.20	±0.05
Q09	Ground Pad Alley, Group 1 to Centerline	12.40	±0.05
Q10	Ground Pad Alley, Group 2 to Centerline	10.80	±0.05
Q11	Ground Pad Alley Spacing	2.40	±0.05
Q12	Ground Pad Alley Width	1.50	±0.05

5.5.4. Electrical Requirements

. Table 5-27 lists the electrical performance requirements for PCI Express x16 mated board and cable connectors.

Table 5-27: x16 Connector Electrical Performance Requirements

Symbol	Parameter	Min	Max	Units	Conditions/Comments
LLCR	Low-Level Contact Resistance - Initial		40	mΩ	
Δ LLCR	Low-Level Contact Resistance - Change		10	mΩ	
ESDV	ESD Performance	2k		V	See Section 3.4

5.5.5. Current and Voltage Rating Requirements

Table 5-28 lists contact rating requirements for PCI Express x16 mated board and cable connectors.

Table 5-28: x16 Current and Voltage Rating Requirements

Symbol	Parameter	Rating	Units	Notes
I_{max}	Contact Current Rating	0.5	A	1
V	Operating Voltage Rating	30	V	

Notes:

1. 30 °C maximum temperature rise and 55 °C maximum ambient per ANSI/EIA-364-70.

5.5.6. Mechanical Requirements

Table 5-29 lists the mechanical performance requirements for PCI Express x16 board connectors.

Table 5-29: x16 Connector Physical and Mechanical Performance Requirements

Symbol	Parameter	Min	Max	Units	Conditions/Comments
F_i	Insertion Force		170	N	
T_w	Withdrawal Force	34		N	
F_r	Retention Force		100	N	
F_{ls}	Side Load Capability		75	N	
F_{ll}	Longitudinal Load Capability		100	N	
F_{rc}	Housing Wafer Retention Force	4.45		N	
W_c	Contact Wipe	0.4		mm	

Notes:

The guide rail is required to be nickel plated.

5.6. Connector Durability

Table 5-30 defines the durability (insertion and withdrawal) cycle requirements for PCI Express external cabling connectors. It is recommended that the contacts be plated with a minimum of 0.76 µm (30 µinches) of gold over 1.27 µm of nickel to achieve the required durability performance.

Table 5-30: Connector Durability Requirements

Cable Link Width	Durability Cycles
x1	1500
x4	250
x8	250
x16	250

5.7. Environmental Performance

It is recommended that board and cable connectors to be used in PCI Express Subsystems be tested in accordance with EIA 364.1000-01, using the appropriate test sequences and the following field life conditions:

- 50 mating cycles preconditioning
- Unmated exposure, option 2 mixed flowing gas exposure
- Five year product life
- Field operating temperature range from -40 °C to 60 °C

6

6. Cable Specification

6.1. Cable Configuration

6.1.1. x1 Cable Assembly

Figure 6-1 shows the PCI Express x1 cable assembly in an isometric view.

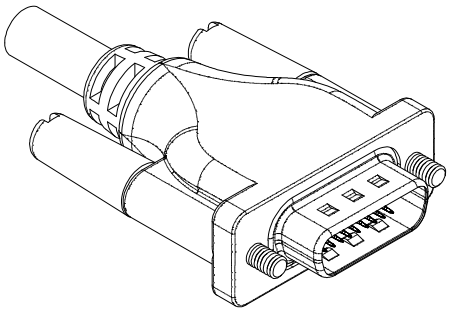
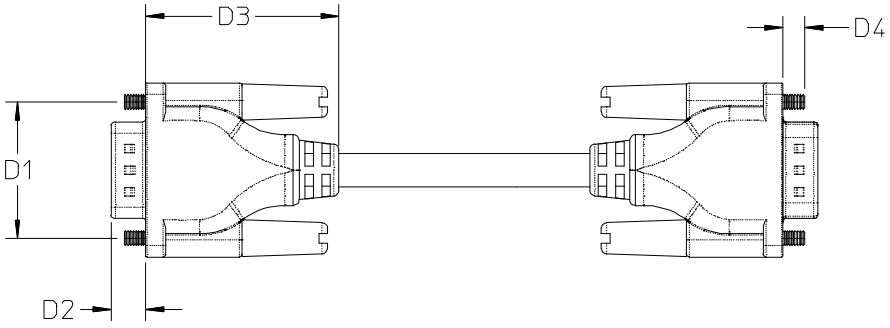


Figure 6-1: x1 Cable Assembly



Notes:
1. Jackpost thread is to be 4-40 UNC-2A.

Figure 6-2: x1 Cable Assembly Top View

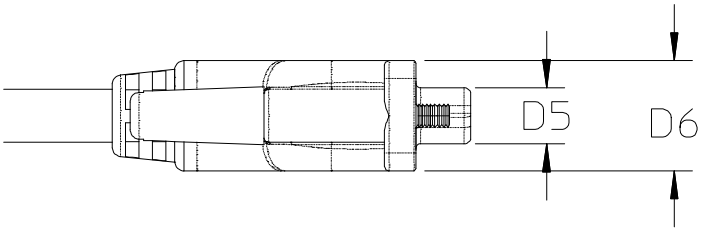


Figure 6-3: x1 Cable Assembly Side View

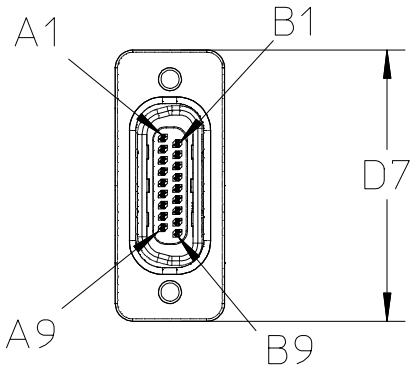


Figure 6-4: x1 Cable Assembly Pin-Out

Table 6-1: x1 Cable Assembly Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
D1	Center to Center Distance of Jack Screws	24.13	± 0.40
D2	Shell Length	6.15	± 0.40
D3	Overmold Length	34.00	± 1.00
D4	Jack Screw Extension	5.10	± 0.50
D5	Shell Height	6.32	± 0.40
D6	Overmold Height	11.75	± 1.00
D7	Overmold Width	30.50	± 0.70

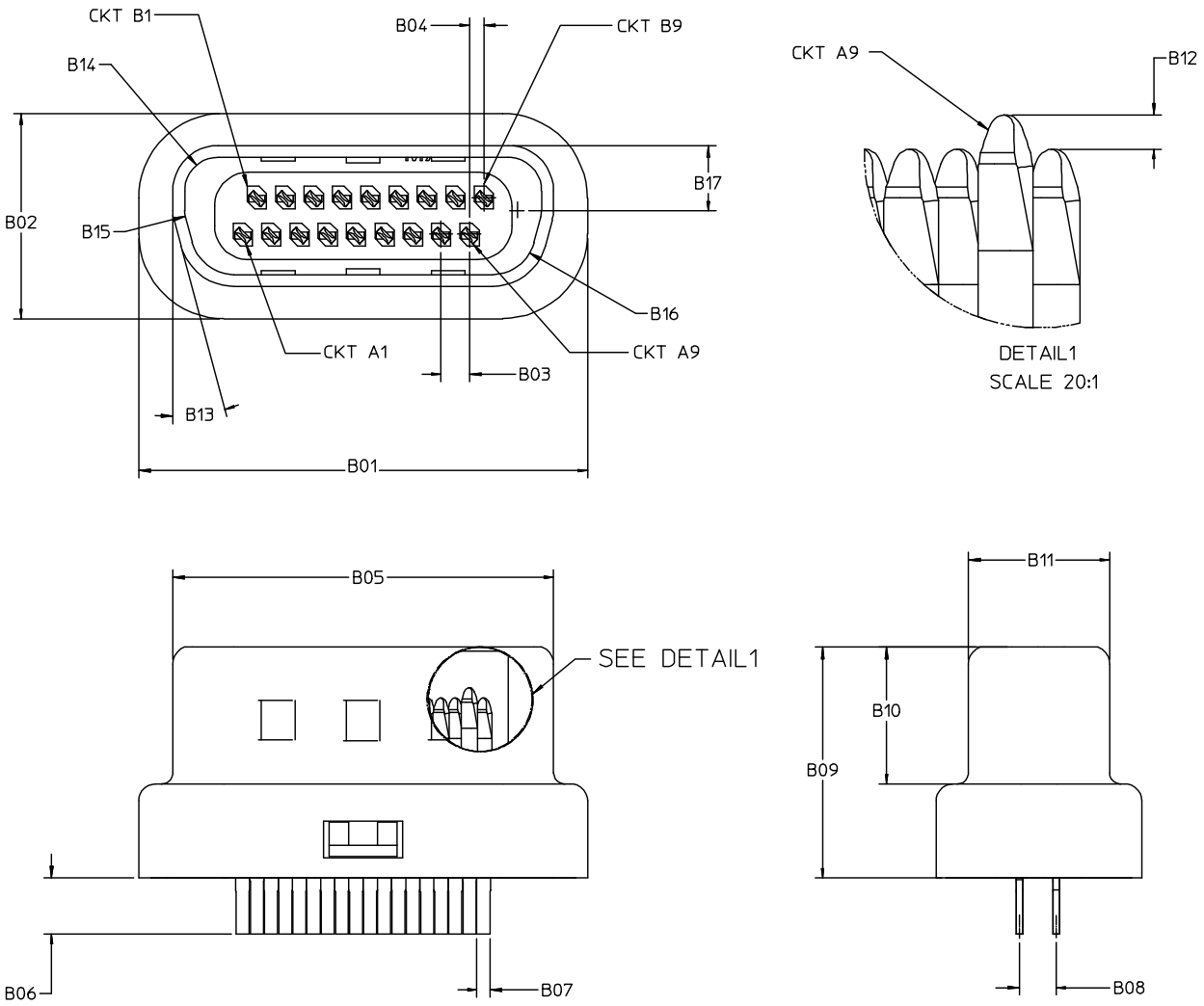


Figure 6-5: x1 Cable Assembly Form Factor

Table 6-2: x1 Cable Assembly Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
B01	OAW of Assembly	20.12	±0.13
B02	OAL of Assembly	9.22	±0.13
B03	Contact Pitch Within Row	1.27	±0.13
B04	Contact Pitch - Row to Row	0.64	±0.13
B05	D Shell Width	17.07	±0.13
B06	Tail Length	2.53	±0.25
B07	Tail Width	0.58	±0.13
B08	Distance Between Rows of Tails	1.65	±0.25
B09	OAH of Shield	10.36	±0.13
B10	D Shell Height	6.15	±0.13
B11	D Shell Length	6.32	±0.13
B12	First Mate-Last Break Dimension	0.36	Minimum
B13	Angle on D Shell	15°	±0.5°
B14	D Shell Upper Radius	1.5	±0.13
B15	D Shell Middle Radius	1.08	±0.13
B16	D Shell Lower Radius	1.93	±0.13
B17	D Shell Middle Radius Location	2.93	±0.13

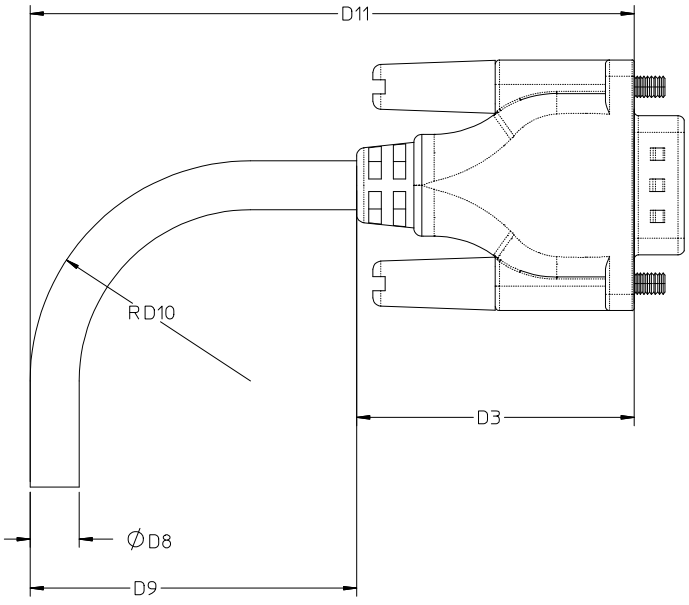


Figure 6-6: x1 Cable Bend Radius

Table 6-3: x1 Cable Bend Radius Dimensions

Designator	24 AWG Dimension (mm)	28 AWG Dimension (mm)	Tolerance (mm)	Description
D3	34.00	34.00	Ref	Overmold Length
D8	6.50	5.80	Ref	Cable Diameter
D9	35.60	32.45	Min	Outer Radius to Rear of Connector
D10	29.25	26.10	Min	Outer Radius
D11	69.60	66.45	Min	Outer Radius to Face of Overmold

Table 6-4: x1 Cable Side Wire Connections

Pin#	Cable Side 1		Cable Side 2	Pin#
A1	PERn0	Differential Pair	PETn0	B8
A2	PERp0		PETp0	B9
A3	reserved	NW	reserved	A3
A4	SB_RTN	Hook-up Wire	SB_RTN	A4
A5	CREFCLKn	Differential Pair	CREFCLKn	A5
A6	CREFCLKp		CREFCLKp	A6
A7	PWR_RTN	NW	PWR_RTN	A7
A8	CPERST#	Hook-up Wire	CPERST#	A8
A9	GND	Drain Wires	GND	B1
B1	GND	Drain Wires	GND	A9
B2	reserved	NW	reserved	B2
B3	CWAKE#	Hook-up Wire	CWAKE#	B3
B4	CPRSNT#	Hook-up Wire	CPRSNT#	B4
B5	GND	Drain Wires	GND	B5
B6	PWR	NW	PWR	B6
B7	CPWRON	Hook-up Wire	CPWRON	B7
B8	PETn0	Differential Pair	PERn0	A1
B9	PETp0		PERp0	A2
Backshell	Chassis Ground	Overall Cable Braid	Chassis Ground	Backshell

Note:

NW refers to no wire.

6.1.2. x4 Cable Assembly

Figure 6-7 shows the PCI Express x4 cable assembly in an isometric view.

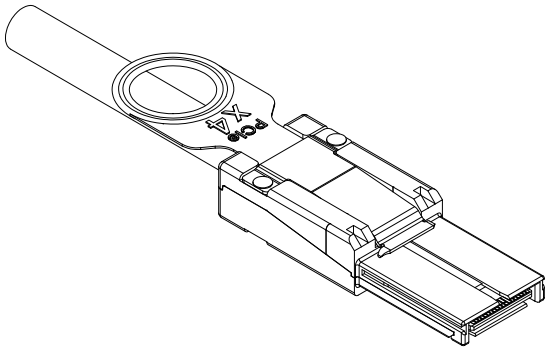


Figure 6-7: x4 Cable Assembly

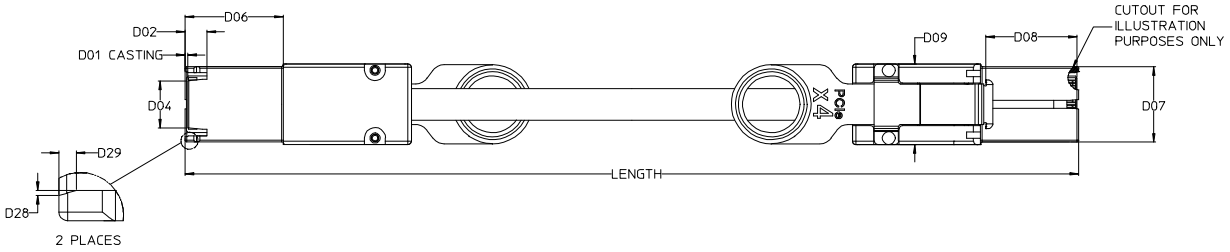


Figure 6-8: x4 Cable Assembly Top and Bottom Views

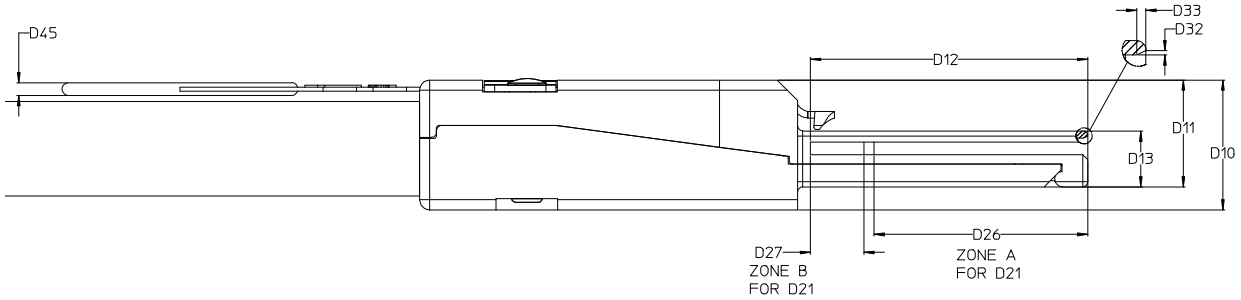


Figure 6-9: x4 Cable Assembly Side View

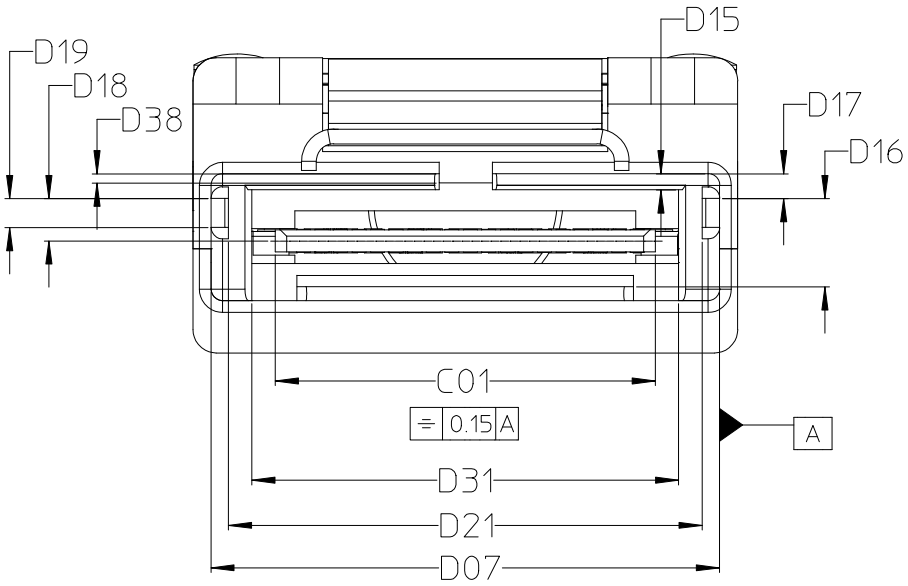


Figure 6-10: x4 Cable Assembly End View

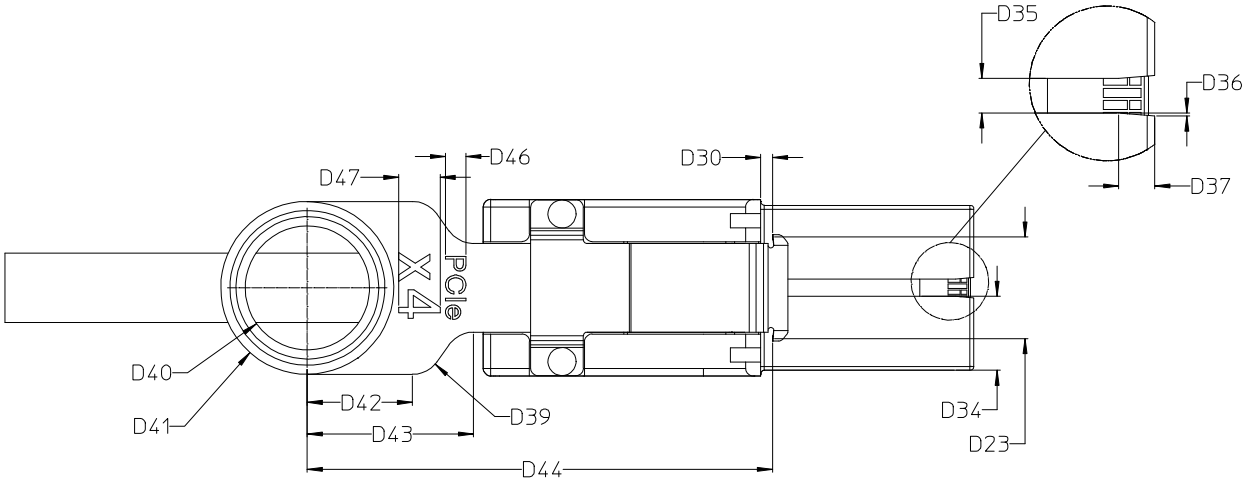


Figure 6-11: x4 Cable Assembly Latch Feature Detail

Notes:
1. PCI Express latch pull tab to be Pantone 354U Green.

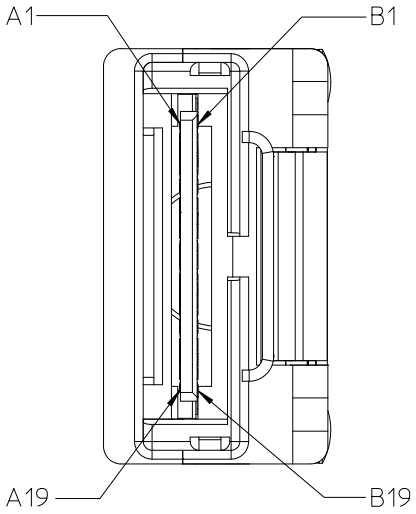


Figure 6-12: x4 Pin Locations

Table 6-5: x4 Cable Side Connector Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
C01	Interface Width	16.40	±0.10
D01	Forward Edge of Plug to Forward Lower Tab	0.75	±0.13
D02	Slot Depth	6.79	±0.13
D04	Forward Lower Tab Width	13.68	±0.13
D06	Snout Length	28.31	±0.13
D07	Snout Width	21.94	+0.20/-0.05
D08	Latch Face Plane to Forward Edge of PCB	26.29	±0.20
D09	Plug Width	23.50	±0.05
D10	Plug Thickness	12.75	±0.13
D11	Top of Plug to Bottom of Snout	10.55	±0.13
D12	Side Rail Groove Length	27.04	±0.13
D13	Snout Thickness	5.54	+0.15/-0.05
D15	Thickness Top Forward Edge of Plug	0.70	±0.05
D16	Top of Rail Groove to Top of Tongue	3.86	+0.15/-0.05
D17	Top of Snout to Top of Side Groove	1.07	±0.05
D18	Top of Side Groove to Centerline of PCB	1.83	±0.13
D19	Side Rail Groove Width	1.25	±0.05
D21 (a)	Internal Width Rail Groove to Rail Groove Zone A	20.44	±0.05
D21 (b)	Internal Width Rail Groove to Rail Groove Zone B	20.74	±0.05
D23	Latch Barb Spacing	13.50	±0.10

Designator	Description	Dimension (mm)	Tolerance (mm)
D26	Length of Zone A	20.84	±0.13
D27	Length of Zone B	5.20	±0.13
D28	Chamfer Width	0.30	±0.05
D29	Chamfer Length	1.00	±0.05
D30	Latch to Plug Body	1.60	±0.13
D31	Internal Plug Width	18.52	±0.10
D32	Chamfer Height	0.20	±0.05
D33	Chamfer Width	0.45	Min
D34	Key Location	9.84	±0.10
D35	Key Width	2.30	±0.10
D36	Chamfer Height	0.20	±0.10
D37	Chamfer Width	2.40	±0.10
D38	Key Depth	0.40	±0.10
D39	Pull Radius	4.00	±0.10
D40	Pull Inner Diameter	16.52	Min
D41	Pull Outer Diameter	23.02	Max
D42	Pull Centerline to Radius	13.97	±0.10
D43	Pull Centerline to Radius	22.09	±0.10
D44	Pull Centerline to Latch	61.82	±3.00
D45	Pull Thickness	1.25	Min
D46	Text Height - PCIe	2.70	Ref
D47	Text Height - x4	5.50	Ref

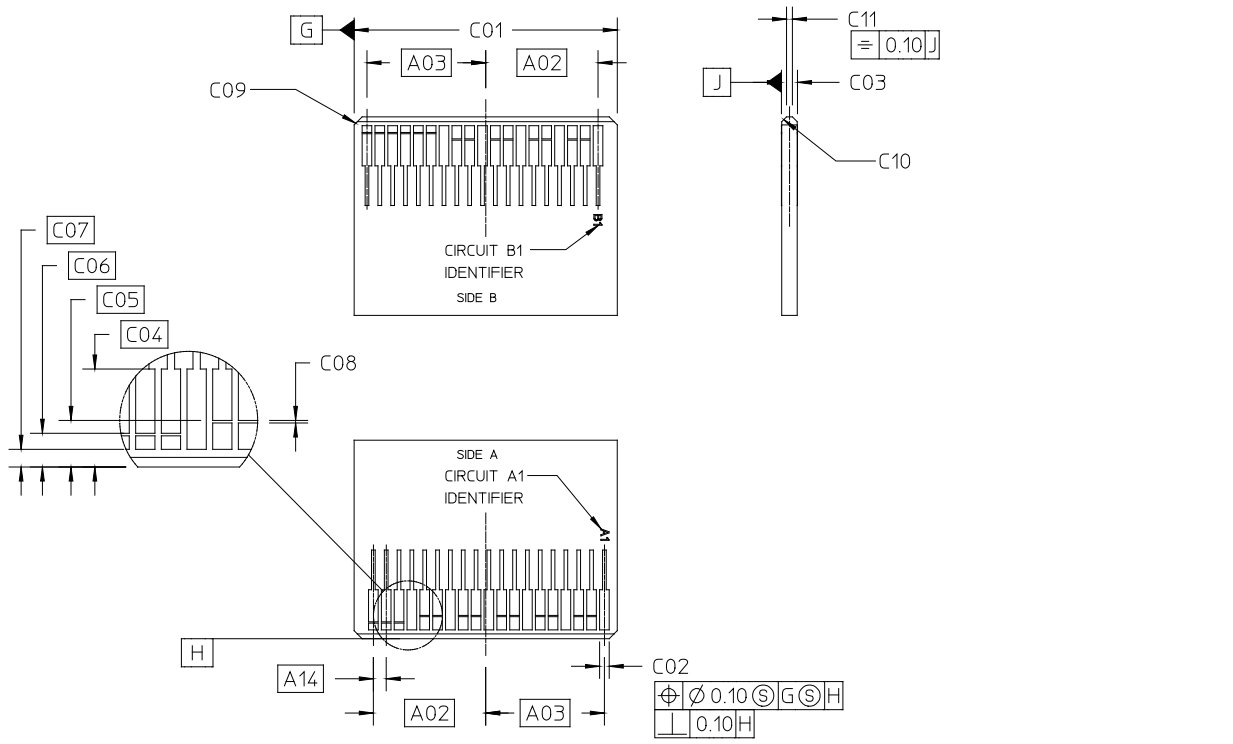


Figure 6-13: x4 Cable Side Connector Module Interface

Table 6-6: x4 Cable Side Connector Module Interface Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
A02	CL to First	7.00	Basic
A03	CL to Last	7.40	Basic
A14	Tail Pitch Within Row	0.80	Basic
C01	Interface Width	16.40	±0.10
C02	Pad Width	0.60	±0.05
C03	PCB Thickness	1.00	±0.10
C04	End of Pad	3.05	±0.10
C05	Third Mate	1.45	±0.10
C06	Second Mate	1.05	±0.10
C07	First Mate	0.55	±0.10

Designator	Description	Dimension (mm)	Tolerance (mm)
C08	Gap Between Mating Levels	0.08	±0.015
C09	Card Slot Chamfer	0.50	±0.13
C10	Mating Chamfer	0.30	±0.10
C11	Lead-in Flat	0.36	Ref

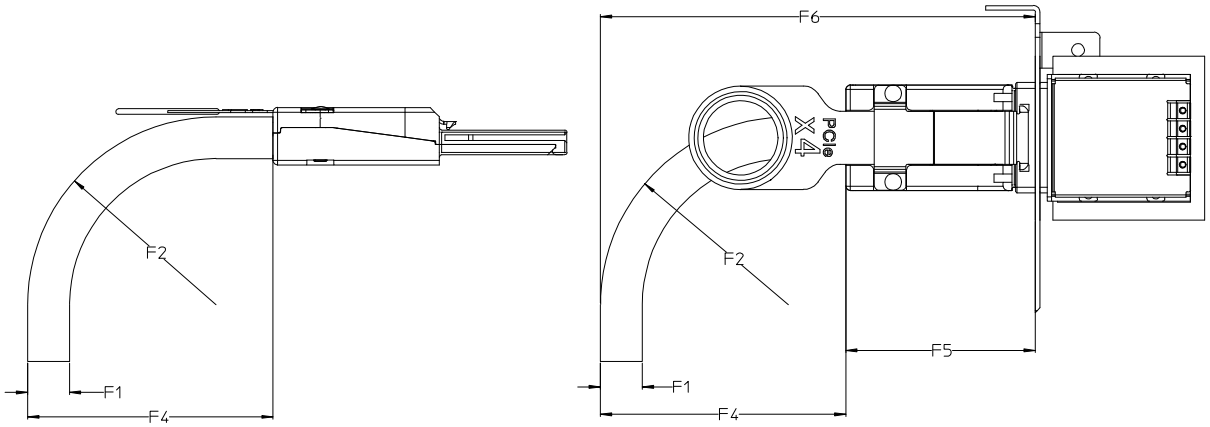


Figure 6-14: x4 Cable Bend Radius

Table 6-7: x4 Cable Bend Radius Dimensions

Designator	24 AWG Dimension (mm)	26 AWG Dimension (mm)	28 AWG Dimension (mm)	Tolerance (mm)	Description
F1	10.40	9.30	8.40	Ref	Cable Diameter
F2	46.90	41.70	37.70	Min	Outer Radius
F4	59.60	54.40	50.40	Min	Outer Radius to Rear of Connector
F5	42.03	42.03	42.03	Basic	Rear of Plug to Faceplate
F6	101.63	96.43	92.43	Min	Faceplate to Outer Radius

Notes:

1. Bend radius is 4x nominal cable diameter.
2. Outer radius is bend radius plus ½ of nominal cable diameter.

Table 6-8: x4 Cable Wire Connections

Pin #	Cable Side 1		Cable Side 2	Pin #
A1 A4 A7 A10 A13 A16 B1 B4 B7 B10 B13	GND	Drain Wires	GND	A1 A4 A7 A10 A13 A16 B1 B4 B7 B10 B13
A2	PETp0	Differential Pair	PERp0	B2
A3	PETn0		PERn0	B3
A5	PETp1	Differential Pair	PERp1	B5
A6	PETn1		PERn1	B6
A8	PETp2	Differential Pair	PERp2	B8
A9	PETn2		PERn2	B9
A11	PETp3	Differential Pair	PERp3	B11
A12	PETn3		PERn3	B12
A14	CREFCLKp	Differential Pair	CREFCLKp	A14
A15	CREFCLKn		CREFCLKn	A15
A17	SB_RTN	Hook-up Wire	SB_RTN	A17
A18	CPRSNT#	Hook-up Wire	CPRSNT#	A18
A19	CPWRON	Hook-up Wire	CPWRON	A19
B2	PERp0	Differential Pair	PETp0	A2
B3	PERn0		PETn0	A3
B5	PERp1	Differential Pair	PETp1	A5
B6	PERn1		PETn1	A6
B8	PERp2	Differential Pair	PETp2	A8
B9	PERn2		PETn2	A9
B11	PERp3	Differential Pair	PETp3	A11
B12	PERn3		PETn3	A12
B14	PWR	NW	PWR	B14
B15	PWR	NW	PWR	B15
B16	PWR_RTN	NW	PWR_RTN	B16
B17	PWR_RTN	NW	PWR_RTN	B17
B18	CWAKE#	Hook-up Wire	CWAKE#	B18
B19	CPERST#	Hook-up Wire	CPERST#	B19
Backshell	Chassis Ground	Overall Cable Braid	Chassis Ground	Backshell

Notes:

NW refers to no wire.

6.1.3. x8 Cable Assembly

A PCI Express x8 cable assembly utilizes the x8 wide connector definition; refer to Section 5.4. Cable bend radius and usability are maintained through implementation of two x4 raw cables for a x8 cable assembly. The two x4 raw cables provide connectivity from end to end for eight PCI Express Lanes and sideband signals. An isometric view of the cable assembly is shown in Figure 6-15.

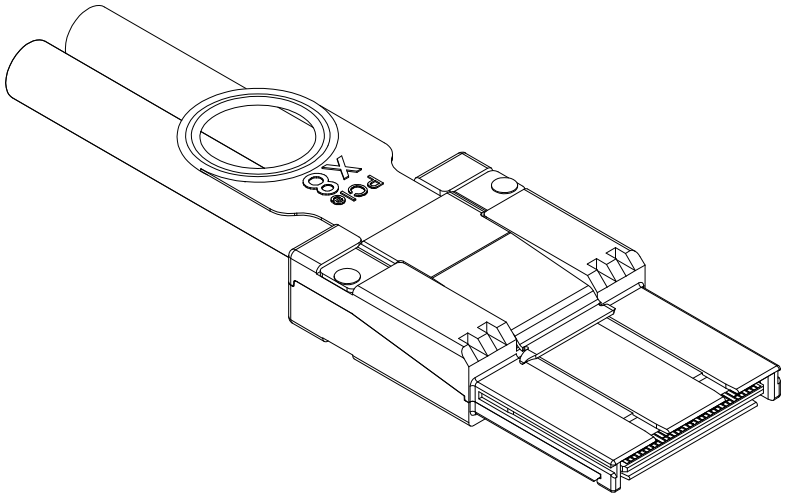


Figure 6-15: x8 Cable Assembly

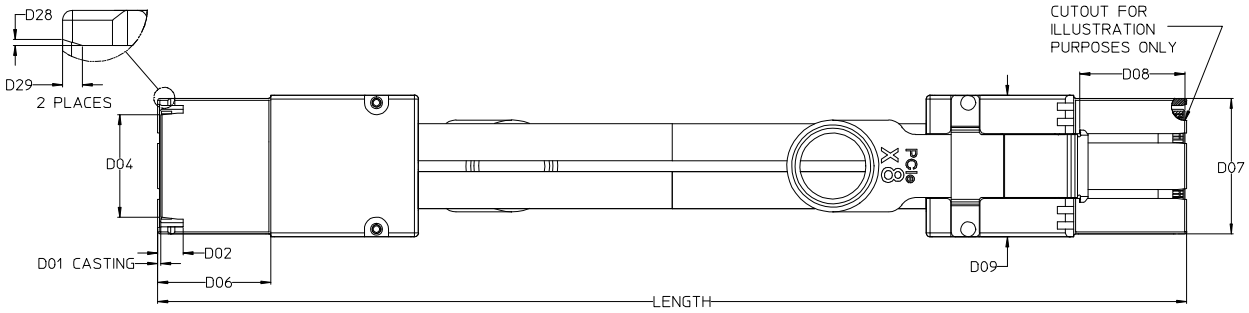


Figure 6-16: x8 Cable Assembly Top and Bottom Views

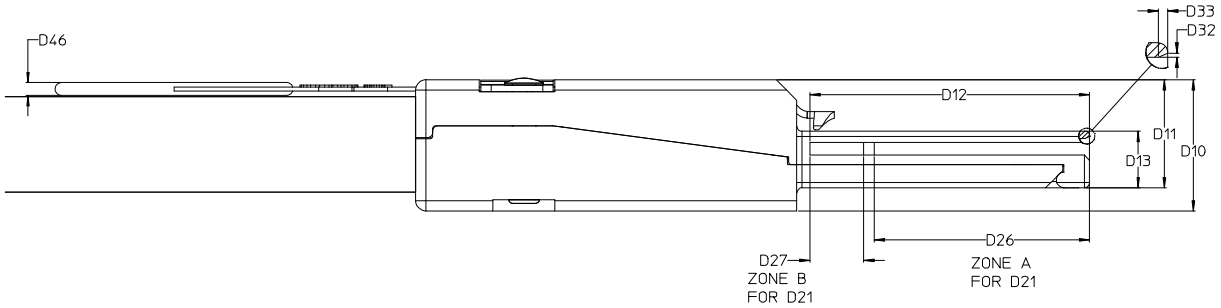


Figure 6-17: x8 Cable Assembly Side View

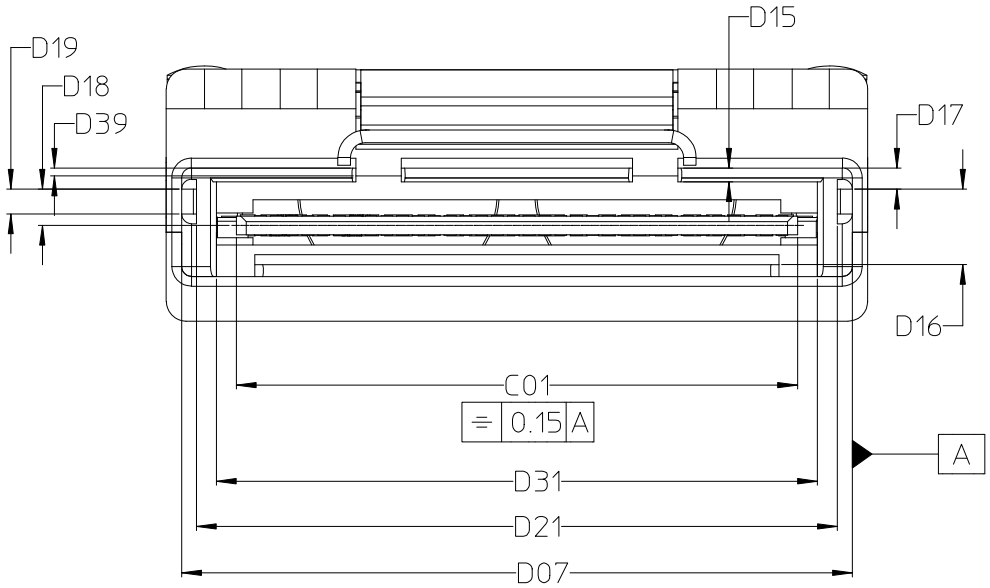
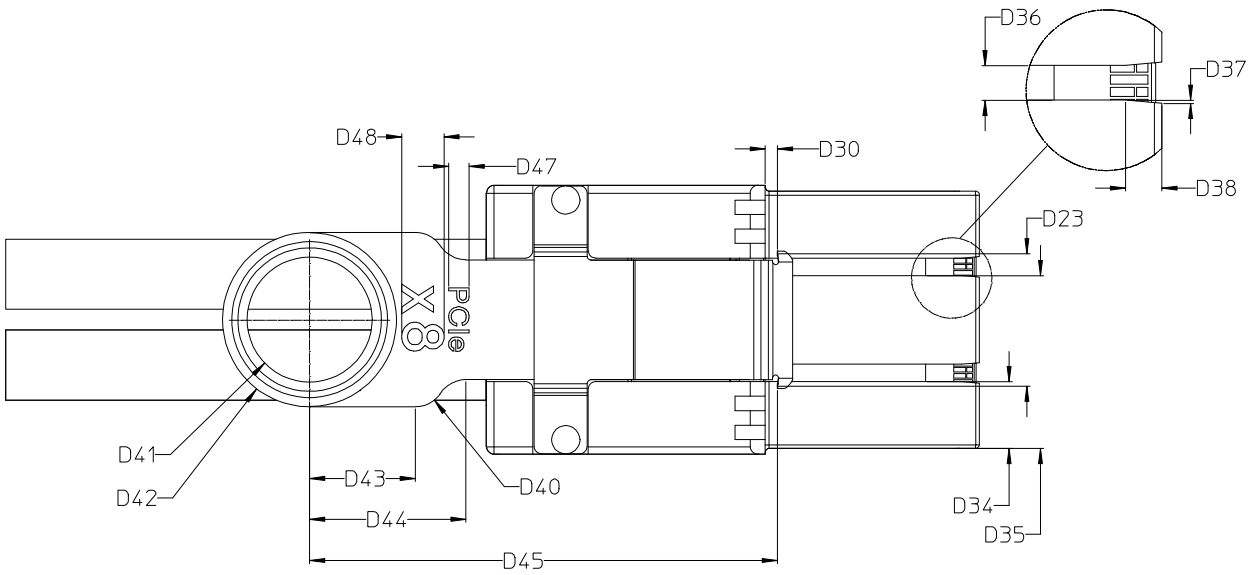


Figure 6-18: x8 Cable Assembly End View



Notes:
1. PCI Express latch pull tab to be Pantone 354U Green.

Figure 6-19: x8 Cable Assembly Latch Feature Detail

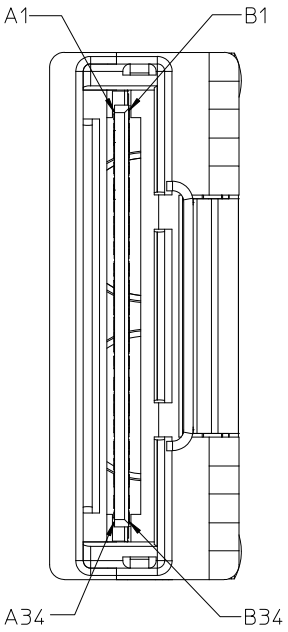


Figure 6-20: x8 Pin Locations

Table 6-9: x8 Cable Side Connector Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
C01	Interface Width	28.40	±0.10
D01	Forward Edge of Plug to Forward Lower Tab	0.75	±0.13
D02	Slot Depth	6.79	±0.13
D04	Forward Lower Tab Width	25.68	±0.13
D06	Snout Length	28.31	±0.13
D07	Snout Width	33.94	+0.20/-0.05
D08	Latch Face Plane to Forward Edge of PCB	26.29	±0.20
D09	Plug Width	35.50	±0.05
D10	Plug Thickness	12.75	±0.13
D11	Top of Plug to Bottom of Snout	10.49	±0.13
D12	Side Rail Groove Length	27.04	±0.13
D13	Snout Thickness	5.54	+0.15/-0.05
D15	Thickness Top Forward Edge of Plug	0.70	±0.05
D16	Top of Rail Groove to Top of Tongue	3.86	+0.15/-0.05
D17	Top of Snout to Top of Side Groove	1.07	±0.05
D18	Top of Side Groove to Centerline of PCB	1.83	±0.13
D19	Side Rail Groove Width	1.25	±0.05
D21	Zone A Internal Width Rail Groove to Rail Groove	32.44	±0.05
D21	Zone B Internal Width Rail Groove to Rail Groove	32.74	±0.05
D23	Latch Barb Spacing	17.50	±0.05
D26	Length of Zone A	20.84	±0.13
D27	Length of Zone B	5.20	±0.13
D28	Chamfer Width	0.30	±0.05
D29	Chamfer Length	1.00	±0.05
D30	Latch to Plug Body	1.60	±0.13
D31	Internal Plug Width	30.42	±0.10
D32	Chamfer Height	0.20	±0.05
D33	Chamfer Width	0.45	Min
D34	Key Location	8.82	±0.10
D35	Key Location	22.82	±0.10
D36	Key Width	2.30	±0.10
D37	Chamfer Height	0.20	±0.10

Designator	Description	Dimension (mm)	Tolerance (mm)
D38	Chamfer Width	2.40	±0.10
D39	Key Depth	0.40	±0.10
D40	Pull Radius	4.00	±0.10
D41	Pull Inner Diameter	16.52	Min
D42	Pull Outer Diameter	23.02	Max
D43	Pull Centerline to Radius	13.97	±0.10
D44	Pull Centerline to Radius	20.67	±0.10
D45	Pull Centerline to Latch	61.82	±3.00
D46	Pull Thickness	1.25	Min
D47	Text Height - PCIe	2.70	Ref
D48	Text Height - x8	5.60	Ref

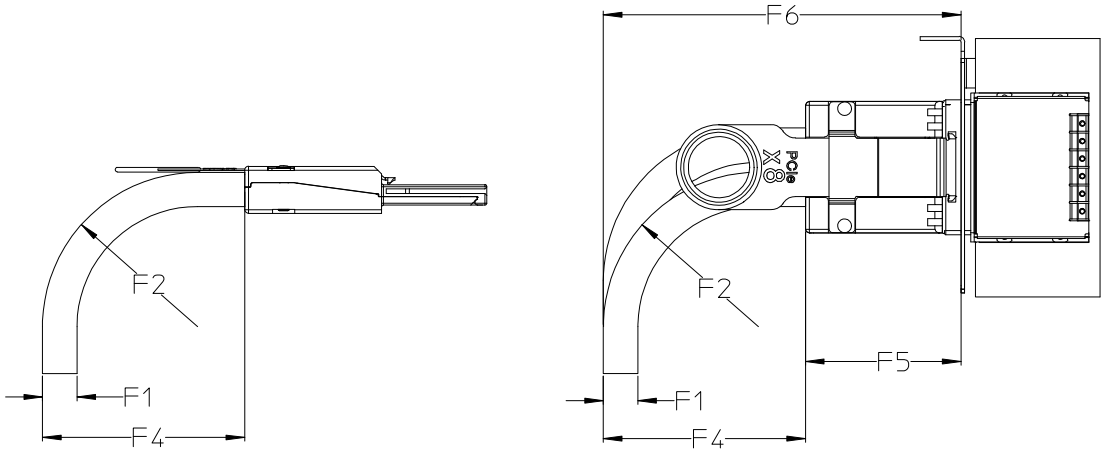


Figure 6-21: x8 Cable Bend Radius

Table 6-10: x8 Cable Bend Radius Dimensions

Designator	24 AWG Dimension (mm)	26 AWG Dimension (mm)	28 AWG Dimension (mm)	Tolerance (mm)	Description
F1	10.40	9.30	8.40	Ref	Cable Diameter
F2	46.90	41.70	37.70	Min	Outer Radius
F4	59.60	54.40	50.40	Min	Outer Radius to Rear of Connector
F5	42.03	42.03	42.03	Basic	Rear of Plug to Faceplate
F6	101.63	96.43	92.43	Min	Faceplate to Outer Radius

Notes:

1. Bend radius is 4x normal cable diameter.
2. Outer radius is bend radius plus ½ of normal cable diameter.

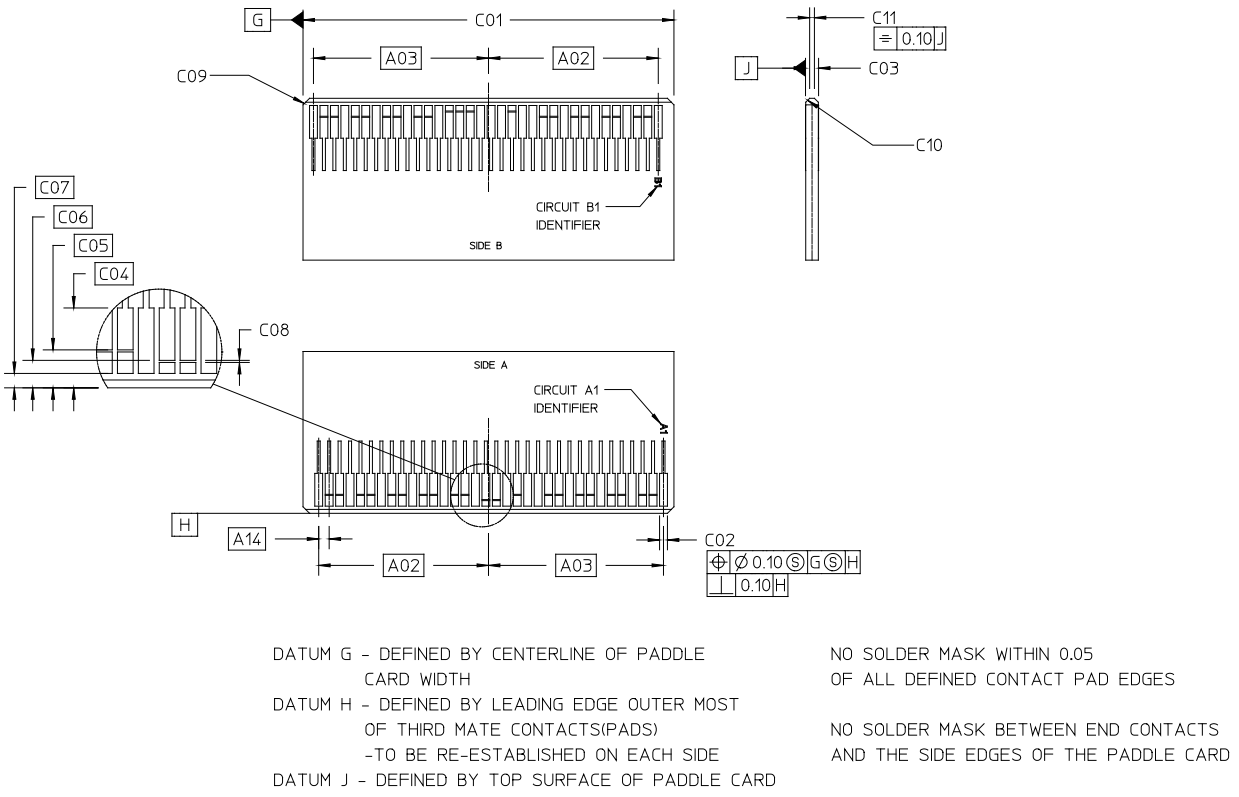


Figure 6-22: x8 Cable Side Connector Module Interface

Table 6-11: x8 Cable Side Connector Module Interface Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
A02	CL to First	13.00	Basic
A03	CL to Last	13.40	Basic
A14	Tail Pitch Within Row	0.80	Basic
C01	Interface Width	28.40	±0.10
C02	Pad Width	0.60	±0.05
C03	PCB Thickness	1.00	±0.10
C04	End of Pad	3.05	±0.10
C05	Third Mate	1.45	±0.10
C06	Second Mate	1.05	±0.10
C07	First Mate	0.55	±0.10
C08	Gap Between Mating Levels	0.08	±0.015
C09	Card Slot Chamfer	0.50	±0.13
C10	Mating Chamfer	0.30	±0.10
C11	Lead-in Flat	0.36	Ref

Table 6-12: x8 Cable Wire Connections

Pin #	Cable Side A		Cable Side B	Pin #
A1 A4 A7 A10 A13 A16 A22 A25 A28 A31 A34 B1 B4 B7 B10 B13 B22 B25 B28 B31 B34	GND	Drain Wires	GND	A1 A4 A7 A10 A13 A16 A22 A25 A28 A31 A34 B1 B4 B7 B10 B13 B22 B25 B28 B31 B34
A2	PETp0	Differential Pair	PERp0	B2
A3	PETn0		PERn0	B3
A5	PETp1	Differential Pair	PERp1	B5
A6	PETn1		PERn1	B6
A8	PETp2	Differential Pair	PERp2	B8
A9	PETn2		PERn2	B9
A11	PETp3	Differential Pair	PERp3	B11
A12	PETn3		PERn3	B12
A14	CREFCLKp	Differential Pair	CREFCLKp	A14
A15	CREFCLKn		CREFCLKn	A15
A17	RSVD	NC	RSVD	A17
A18	RSVD	NC	RSVD	A18

Pin #	Cable Side A		Cable Side B	Pin #
A19	SB_RTN	Hook-up Wire	SB_RTN	A19
A20	CPRSNT#	Hook-up Wire	CPRSNT#	A20
A21	CPWRON	Hook-up Wire	CPWRON	A21
A23	PETp4	Differential Pair	PERp4	B23
A24	PETn4		PERn4	B24
A26	PETp5	Differential Pair	PERp5	B26
A27	PETn5		PERn5	B27
A29	PETp6	Differential Pair	PERp6	B29
A30	PETn6		PERn6	B30
A32	PETp7	Differential Pair	PERp7	B32
A33	PETn7		PERn7	B33
B2	PERp0	Differential Pair	PETp0	A2
B3	PERn0		PETn0	A3
B5	PERp1	Differential Pair	PETp1	A5
B6	PERn1		PETn1	A6
B8	PERp2	Differential Pair	PETp2	A8
B9	PERn2		PETn2	A9
B11	PERp3	Differential Pair	PETp3	A11
B12	PERn3		PETn3	A12
B14	PWR	NW	PWR	B14
B15	PWR	NW	PWR	B15
B16	PWR	NW	PWR	B16
B17	PWR_RTN	NW	PWR_RTN	B17
B18	PWR_RTN	NW	PWR_RTN	B18
B19	PWR_RTN	NW	PWR_RTN	B19
B20	CWAKE#	Hook-up Wire	CWAKE#	B20
B21	CPERST#	Hook-up Wire	CPERST#	B21
B23	PERp4	Differential Pair	PETp4	A23
B24	PERn4		PETn4	A24
B26	PERp5	Differential Pair	PETp5	A26
B27	PERn5		PETn5	A27
B29	PERp6	Differential Pair	PETp6	A29
B30	PERn6		PETn6	A30

Pin #	Cable Side A		Cable Side B	Pin #
B32	PERp7	Differential Pair	PETp7	A32
B33	PERn7		PETn7	A33
Backshell	Chassis Ground	Overall Cable Braid	Backshell	Chassis Ground

Notes:

1. NW refers to No Wire. The cable bundle(s) shall not provide wires for power distribution.
2. NC refers to No Connect. These pins are reserved for future use and not connected at the Subsystem or cable assembly.

6.1.4. x16 Cable Assembly

A PCI Express x16 cable assembly utilizes the x16 wide connector definition; refer to Section 5.5. Cable bend radius and usability are maintained through implementation of four x4 raw cables for a x16 cable assembly. The four x4 raw cables provide connectivity from end to end for 16 PCI Express Lanes and sideband signals. The cable wire connections, provided in Table 6-16, include two sets of sideband signals. Only one set is actually implemented at the Upstream and Downstream Subsystem. Having two sets of wires for sideband signals allows the cable assembly to function without requiring keying. Refer to Section 5.5 for additional details on this implementation. The width of the mating interface is reduced by defining a x16 cable assembly as two x8 cable assemblies contained within a common backshell. An isometric view of the cable assembly is shown in Figure 6-23.

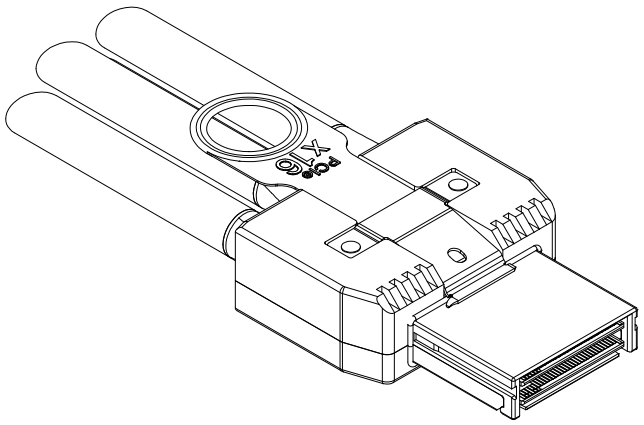


Figure 6-23: x16 Cable Assembly

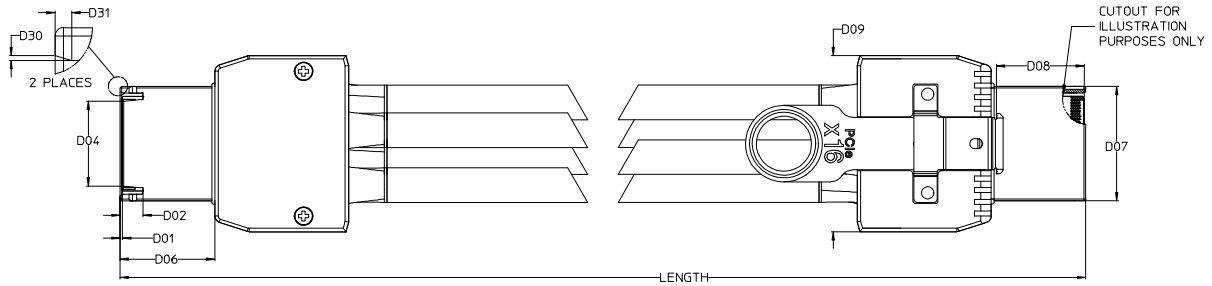


Figure 6-24: x16 Cable Assembly Top and Bottom Views

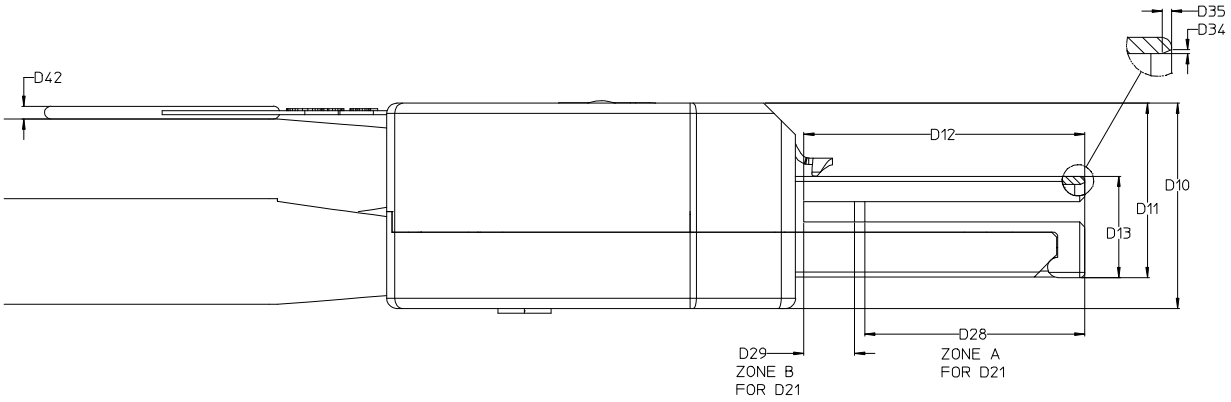


Figure 6-25: x16 Cable Assembly Side View

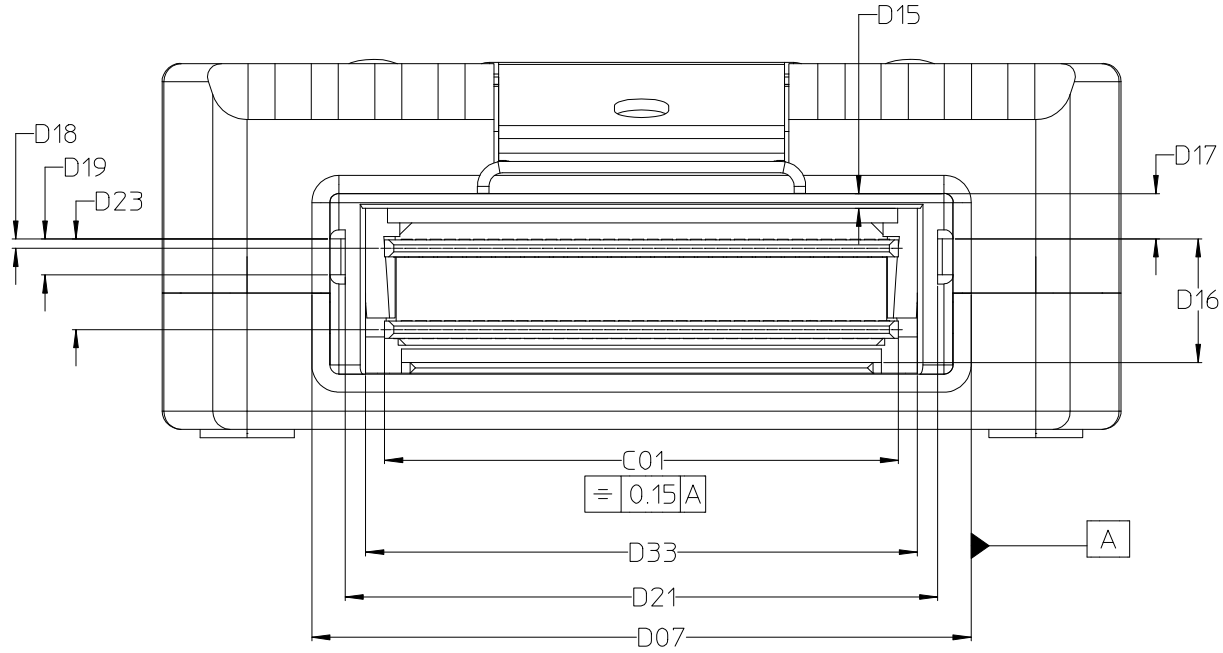
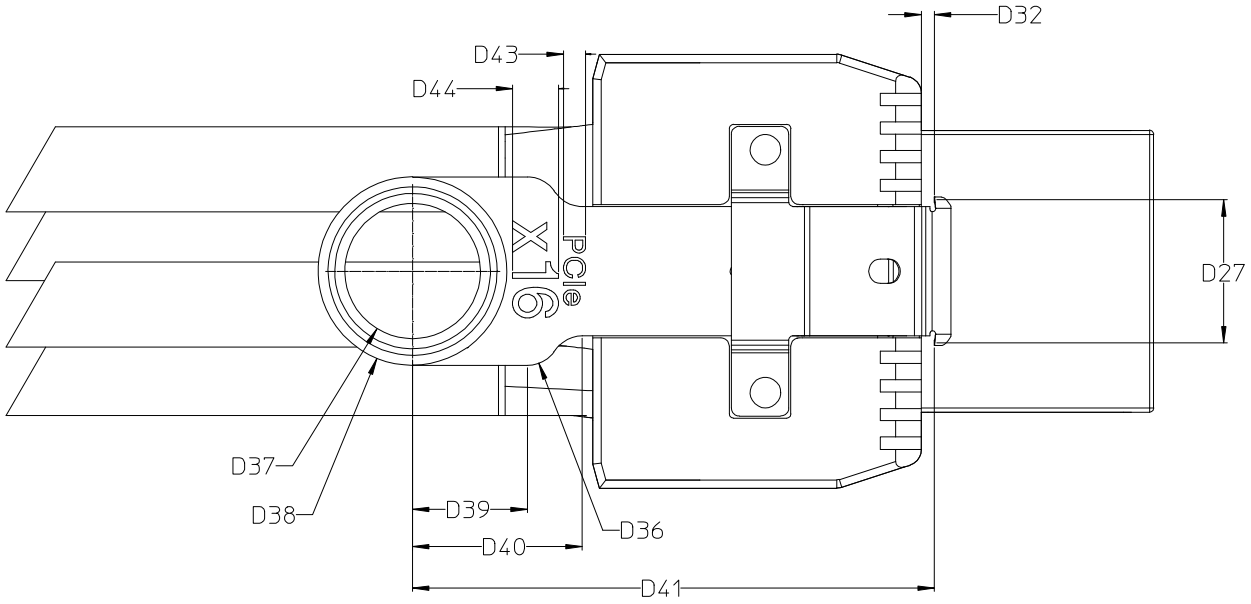


Figure 6-26: x16 Cable Assembly End View



Notes:
1. PCI Express latch pull tab to be Pantone 354U Green.

Figure 6-27: x16 Cable Assembly Latch Feature Detail

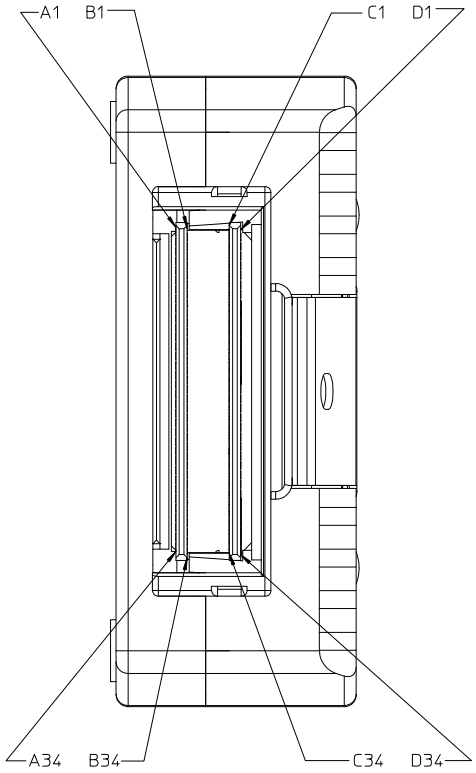


Figure 6-28: x16 Pin Locations

Table 6-13: x16 Cable Side Connector Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
C01	Interface Width	28.40	±0.10
D01	Forward Edge of Plug to Forward Lower Tab	0.75	±0.13
D02	Slot Depth	6.79	±0.13
D04	Forward Lower Tab Width	25.53	±0.13
D06	Snout Length	28.31	±0.13
D07	Snout Width	34.44	+0.20/-0.05
D08	Latch Face Plane to Forward Edge of PCB	26.29	±0.20
D09	Plug Width	53.00	±0.05
D10	Plug Thickness	20.23	±0.13
D11	Top of Plug to Bottom of Snout	17.18	±0.13
D12	Side Rail Groove Length	27.60	±0.10
D13	Snout Thickness	9.99	+0.15/-0.05
D15	Thickness Top Forward Edge of Plug	0.80	±0.05
D16	Top of Rail Groove to Top of Tongue	6.83	+0.15/-0.05
D17	Top of Snout to Top of Side Groove	2.50	±0.05
D18	Top of Side Groove to Centerline of Upper PCB	0.53	±0.13
D19	Side Rail Groove Width	2.05	±0.05
D21	Zone A Internal Width Rail Groove to Rail Groove	33.24	±0.05
D21	Zone B Internal Width Rail Groove to Rail Groove	32.74	±0.05
D23	Top of Side Groove to Centerline of Lower PCB	5.03	±0.13
D27	Latch Barb Spacing	17.50	±0.05
D28	Length of Zone A	21.54	±0.13
D29	Length of Zone B	5.00	±0.13
D30	Chamfer Width	0.30	±0.05
D31	Chamfer Length	1.00	±0.05
D32	Latch to Plug Body	1.60	±0.13
D33	Internal Plug Width	30.55	±0.10
D34	Chamfer Height	0.20	±0.05
D35	Chamfer Width	0.45	Min
D36	Pull Radius	4.00	±0.10
D37	Pull Inner Diameter	16.52	Min
D38	Pull Outer Diameter	23.02	Max

Designator	Description	Dimension (mm)	Tolerance (mm)
D39	Pull Centerline to Radius	13.97	±0.10
D40	Pull Centerline to Radius	20.67	±0.10
D41	Pull Centerline to Latch	63.57	±3.00
D42	Pull Thickness	1.25	Min
D43	Text Height - PCIe	2.70	Ref
D44	Text Height - x16	5.60	Ref

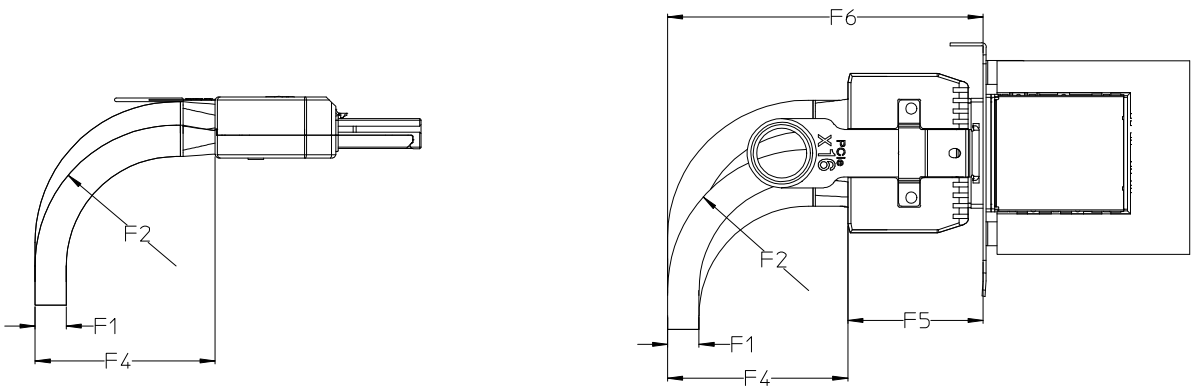


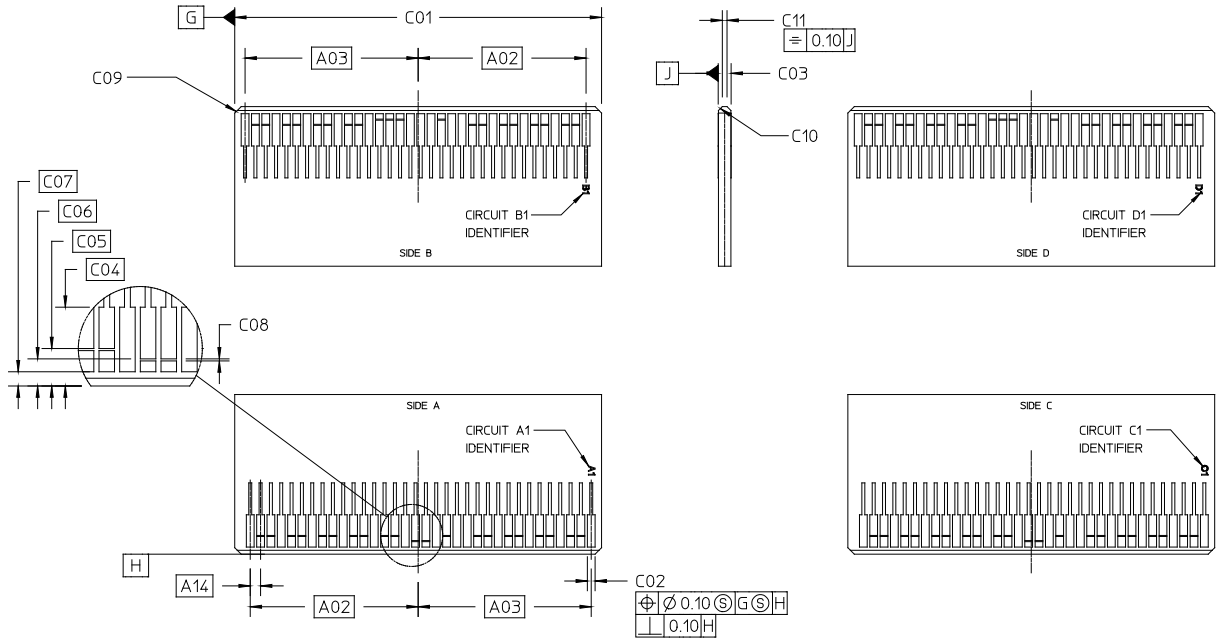
Figure 6-29: x16 Cable Bend Radius

Table 6-14: x16 Cable Bend Radius Dimensions

Designator	24 AWG Dimension (mm)	26 AWG Dimension (mm)	28 AWG Dimension (mm)	Tolerance (mm)	Description
F1	10.4	9.3	8.4	Ref	Cable Diameter
F2	46.9	41.7	37.7	Min	Outer Radius
F4	59.60	54.40	50.40	Min	Outer Radius to Rear of Connector
F5	44.96	44.96	44.96	Basic	Rear of Plug to Faceplate
F6	104.56	99.36	95.36	Min	Faceplate to Outer Radius

Notes:

1. Bend radius is 4x nominal cable diameter.
2. Outer radius is bend radius plus ½ of nominal cable diameter.



DATUM G - DEFINED BY CENTERLINE OF PADDLE CARD WIDTH

DATUM H - DEFINED BY LEADING EDGE OUTER MOST OF THIRD MATE CONTACTS(PADS) -TO BE RE-ESTABLISHED ON EACH SIDE

DATUM J - DEFINED BY TOP SURFACE OF PADDLE CARD

NO SOLDER MASK WITHIN 0.05 OF ALL DEFINED CONTACT PAD EDGES

NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDE EDGES OF THE PADDLE CARD

Figure 6-30: x16 Cable Side Connector Module Interface

Table 6-15: x16 Cable Side Connector Module Interface Dimensions

Designator	Description	Dimension (mm)	Tolerance (mm)
A02	CL to First	13.00	Basic
A03	CL to Last	13.40	Basic
A14	Tail Pitch Within Row	0.80	Basic
C01	Interface Width	28.40	±0.10
C02	Pad Width	0.60	±0.05
C03	PCB Thickness	1.00	±0.10
C04	End of Pad	3.05	±0.10
C05	Third Mate	1.45	±0.10
C06	Second Mate	1.05	±0.10
C07	First Mate	0.55	±0.10
C08	Gap Between Mating Levels	0.08	±0.015
C09	Card Slot Chamfer	0.50	±0.13
C10	Mating Chamfer	0.30	±0.10
C11	Lead-in Flat	0.36	Ref

Table 6-16: x16 Cable Wire Connections

Pin #	Cable Side 1		Cable Side 2	Pin #
A1 A4 A7 A10 A13 A18 A21 A24 A27 A30 A33 B1 B4 B7 B10 B13 B21 B24 B27 B30 B33 C1 C4 C7 C10 C13 C21 C24 C27 C18 C30 C33 D1 D4 D7 D10 D13 D21 D24 D27 D30 D33	GND	Drain Wires	GND	A1 A4 A7 A10 A13 A18 A21 A24 A27 A30 A33 B1 B4 B7 B10 B13 B21 B24 B27 B30 B33 C1 C4 C7 C10 C13 C21 C24 C27 C18 C30 C33 D1 D4 D7 D10 D13 D21 D24 D27 D30 D33
A2	PERp1	Differential Pair	PETp1	C2
A3	PERn1		PETn1	C3
A5	PERp3	Differential Pair	PETp3	C5
A6	PERn3		PETn3	C6
A8	PERp5	Differential Pair	PETp5	C8
A9	PERn5		PETn5	C9
A11	PERp7	Differential Pair	PETp7	C11
A12	PERn7		PETn7	C12
A14	PWR	NW	PWR	A14
A15	PWR	NW	PWR	A15
A16	PWR	NW	PWR	A16
A17	SB_RTN1	Hook-up Wire	SB_RTN1	C17
A19	CREFCLKp1	Differential Pair	CREFCLKp1	C19
A20	CREFCLKn1		CREFCLKn1	C20
A22	PERp9	Differential Pair	PETp9	C22
A23	PERn9		PETn9	C23
A25	PERp11	Differential Pair	PETp11	C25
A26	PERn11		PETn11	C26
A28	PERp13	Differential Pair	PETp13	C28
A29	PERn13		PETn13	C29
A31	PERp15	Differential Pair	PETp15	C31
A32	PERn15		PETn15	C32
A34	RSVD	NC	RSVD	A34
B2	PERp0	Differential Pair	PETp0	D2
B3	PERn0		PETn0	D3

Pin #	Cable Side 1		Cable Side 2	Pin #
B5	PERp2	Differential Pair	PETp2	D5
B6	PERn2		PETn2	D6
B8	PERp4	Differential Pair	PETp4	D8
B9	PERn4		PETn4	D9
B11	PERp6	Differential Pair	PETp6	D11
B12	PERn6		PETn6	D12
B14	PWR_RTN	NW	PWR_RTN	B14
B15	PWR_RTN	NW	PWR_RTN	B15
B16	PWR_RTN	NW	PWR_RTN	B16
B17	CPWRON1	Hook-up Wire	CPWRON1	D17
B18	CWAKE#1	Hook-up Wire	CWAKE#1	D18
B19	CPRSNT#1	Hook-up Wire	CPRSNT#1	D19
B20	CPERST#1	Hook-up Wire	CPERST#1	D20
B22	PERp8	Differential Pair	PETp8	D22
B23	PERn8		PETn8	D23
B25	PERp10	Differential Pair	PETp10	D25
B26	PERn10		PETn10	D26
B28	PERp12	Differential Pair	PETp12	D28
B29	PERn12		PETn12	D29
B31	PERp14	Differential Pair	PETp14	D31
B32	PERn14		PETn14	D32
B34	RSVD	NC	RSVD	B34
C2	PETp1	Differential Pair	PERp1	A2
C3	PETn1		PERn1	A3
C5	PETp3	Differential Pair	PERp3	A5
C6	PETn3		PERn3	A6
C8	PETp5	Differential Pair	PERp5	A8
C9	PETn5		PERn5	A9
C11	PETp7	Differential Pair	PERp7	A11
C12	PETn7		PERn7	A12
C14	PWR	NW	PWR	C14
C15	PWR	NW	PWR	C15
C16	PWR	NW	PWR	C16
C17	SB_RTN2	Hook-up Wire	SB_RTN2	A17

Pin #	Cable Side 1		Cable Side 2	Pin #
C19	CREFCLKp2	Differential Pair	CREFCLKp2	A19
C20	CREFCLKn2		CREFCLKn2	A20
C22	PETp9	Differential Pair	PERp9	A22
C23	PETn9		PERn9	A23
C25	PETp11	Differential Pair	PERp11	A25
C26	PETn11		PERn11	A26
C28	PETp13	Differential Pair	PERp13	A28
C29	PETn13		PERn13	A29
C31	PETp15	Differential Pair	PERp15	A31
C32	PETn15		PERn15	A32
C34	RSVD	NC	RSVD	C34
D2	PETp0	Differential Pair	PERp0	B2
D3	PETn0		PERn0	B3
D5	PETp2	Differential Pair	PERp2	B5
D6	PETn2		PERn2	B6
D8	PETp4	Differential Pair	PERp4	B8
D9	PETn4		PERn4	B9
D11	PETp6	Differential Pair	PERp6	B11
D12	PETn6		PERn6	B12
D14	PWR_RTN	NW	PWR_RTN	D14
D15	PWR_RTN	NW	PWR_RTN	D15
D16	PWR_RTN	NW	PWR_RTN	D16
D17	CPWRON2	Hook-up Wire	CPWRON2	B17
D18	CWAKE#2	Hook-up Wire	CWAKE#2	B18
D19	CPRSNT#2	Hook-up Wire	CPRSNT#2	B19
D20	CPERST#2	Hook-up Wire	CPERST#2	B20
D22	PETp8	Differential Pair	PERp8	B22
D23	PETn8		PERn8	B23
D25	PETp10	Differential Pair	PERp10	B25
D26	PETn10		PERn10	B26
D28	PETp12	Differential Pair	PERp12	B28
D29	PETn12		PERn12	B29
D31	PETp14	Differential Pair	PERp14	B31
D32	PETn14		PERn14	B32

Pin #	Cable Side 1		Cable Side 2	Pin #
D34	RSVD	NC	RSVD	D34
Backshell		Chassis Ground		Backshell

Notes:

1. NW refers to No Wire. The cable bundle(s) shall not provide wires for power distribution.
2. NC refers to No Connect. These pins are reserved for future use and not connected at the Subsystem or cable assembly.
3. The x16 cable assembly includes two copies of sideband signals. This prevents a polarity requirement as the pin-out is different at the Upstream and Downstream Subsystem.

6.2. Requirements

6.2.1. Physical and Mechanical Performance

Mechanical Requirements for x4, x8, and x16:

- Plug bodies are required to be nickel plated.
- Card edge mating pads are recommended to be 0.76 µm minimum hard gold over 3.8 µm nickel.

Additional mechanical requirements are stated in Chapter 5. All Chapter 5 requirements that apply to mated connectors apply to the cable assembly. Table 6-17 lists the cable flex requirements.

Table 6-17: Cable Flex Requirements

Item	Test Condition	Flex Cycles
x1 Cable Assembly	EIA-364-41 Condition 1 Dimension X=3.7 x Cable OD	100
x4 Cable Assembly	EIA-364-41 Condition 1 Dimension X=3.7 x Cable OD	20
x8 Cable Assembly	EIA-364-41 Condition 1 Dimension X=3.7 x Cable OD	20
x16 Cable assembly	EIA-364-41 Condition 1 Dimension X=3.7 x Cable OD	20

6.2.2. Electrical Performance

Note: Values and limits for frequency domain parameters are typically listed in this document as Loss Values, and are therefore positive. However, since they are losses, the actual measured values, either simulated or measured, would be negative. Table 6-18 lists the electrical performance requirements for PCI Express external cables.

Cable assembly compliance testing is accomplished using frequency domain techniques. The insertion loss, return loss, and crosstalk requirements are provided in the following sections. Cable assembly time domain testing may be performed against the eye diagrams in lieu of the frequency domain parameters, further enabling trade-offs between the cable assembly interconnect parameters and implementations such as equalization.

Table 6-18: Cable Assembly Differential Characteristics Summary

Description	Values for 2.5 GT/s	Values for 5.0 GT/s	Unit	Reference
Maximum Insertion Loss at 5.0 GHz	N/A	14.8	dB	Section 6.2.2.1
Maximum Insertion Loss at 2.5 GHz	N/A	9.3		
Maximum Insertion Loss at 1.25 GHz	7.5	5.9		
Maximum Insertion Loss at 625 MHz	5.0	3.9		
Minimum Return Loss at 5.0 GHz	N/A	7.0	dB	Section 6.2.2.2
Minimum Return Loss at 2.5 GHz	N/A	7.0		
Minimum Return Loss at 1.25 GHz	12.0	12.0		
Minimum NEXT Loss at 5.0 GHz	N/A	29.2	dB	Section 6.2.2.3
Minimum NEXT Loss at 2.5 GHz	N/A	33.0		
Minimum NEXT Loss at 1.25 GHz	35.0	36.8		
Minimum MDNEXT Loss at 5.0 GHz	N/A	27.7	dB	Section 6.2.2.4
Minimum MDNEXT Loss at 2.5 GHz	N/A	31.5		
Minimum MDNEXT Loss at 1.25 GHz	31.5	35.3		
Minimum ELFEXT at 5.0 GHz	N/A	21.3	dB	Section 6.2.2.5
Minimum ELFEXT at 2.5 GHz	N/A	27.0		
Minimum ELFEXT at 1.25 GHz	25.08	32.7		
Minimum MDELFEXT at 5.0 GHz	N/A,	17.3	dB	Section 6.2.2.7
Minimum MDELFEXT at 2.5 GHz	N/A,	23.0		
Minimum MDELFEXT at 1.25 GHz	23.08	28.7		
Minimum DCMC below 2.5 GHz	N/A	18.0	dB	Section 6.2.2.10

6.2.2.1. Maximum Insertion Loss

2.5 GT/s

The insertion loss of each pair of the cable assembly shall meet the values determined using Equation (6–1).

$$Insertion\ Loss(f) \leq 0.143\sqrt{f} + 0.0018 \times f + \frac{6.87}{\sqrt{f}} \quad dB \quad 100 \leq f \leq 2500 \qquad (6\text{-}1)$$

where f is the frequency in MHz.

5.0 GT/s

The insertion loss for each pair in a cable assembly operating at 5.0 GT/s shall meet the values using Equation (6-2).

$$InsertionLoss(f) \leq 0.1250\sqrt{f} + 0.0012 \times f \quad dB \quad 100 \leq f \leq 7500 \qquad (6\text{-}2)$$

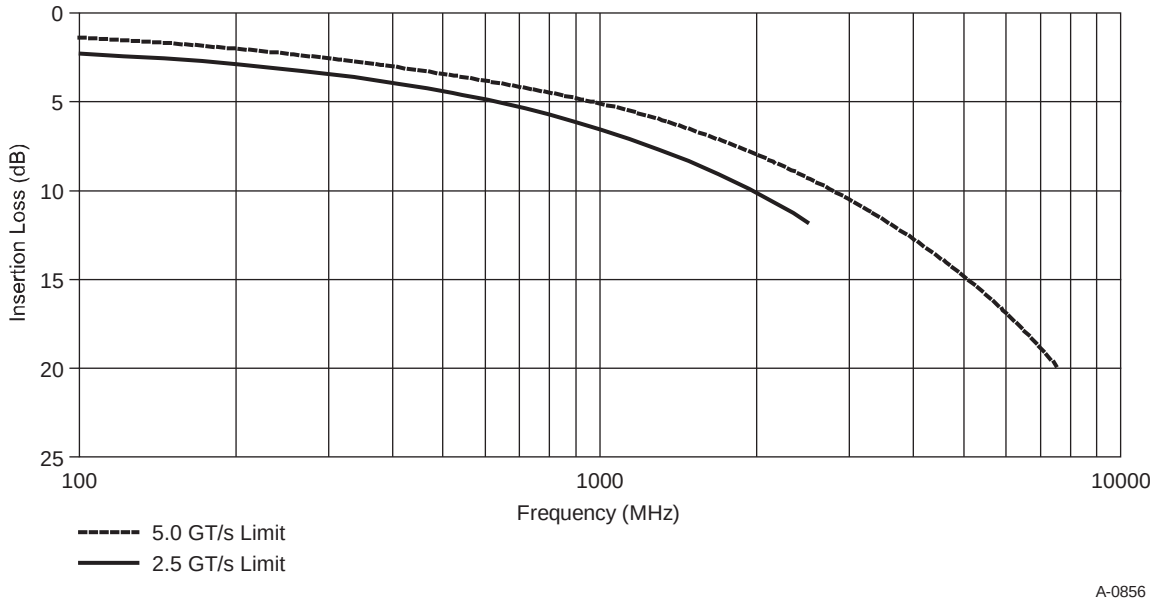


Figure 6-31: Cable Assembly Insertion Loss

Controlling the ISI jitter component through additional equalization within the cable assembly is allowed. Details of such implementations are beyond the scope of this specification.

6.2.2.2. Minimum Return Loss

2.5 GT/s

The return loss of each pair of the cable assembly shall meet the values determined using Equation (6–3).

$$ReturnLoss(f) \geq 12 \quad dB \qquad 100 \leq f(MHz) \leq 2500 \tag{6-3}$$

where f is the frequency in MHz.

5.0 GT/s

The return loss of each pair of the cable assembly shall meet the values determined using Equation (6–4).

$$ReturnLoss(f) \geq 12 \quad dB \qquad 100 \leq f(MHz) \leq 2500 \tag{6-4}$$

$$ReturnLoss(f) \geq 7 \quad dB \qquad 2500 < f(MHz) \leq 7500$$

6.2.2.3. Minimum NEXT Loss

2.5 GT/s

The differential pair-to-pair near-end crosstalk (NEXT) loss between any transmit lane and any receive lane of a cable assembly shall meet the values determined using Equation (6–5+).

$$NextLoss(f) \geq 35 - 17 \times \log\left(\frac{f}{1250}\right) \quad dB \quad 100 \leq f \leq 2500 \tag{6-5}$$

where f is the frequency in MHz.

5.0 GT/s

The differential pair-to-pair near-end crosstalk (NEXT) loss between any transmit lane and any receive lane of a cable assembly shall meet the values determined using Equation (6–6).

$$NextLoss(f) \geq 33.0 - 12.5 \times \log\left(\frac{f}{2500}\right) \quad dB \quad 100 \leq f \leq 7500 \tag{6-6}$$

where f is the frequency in MHz.

6.2.2.4. Minimum Multiple Disturber NEXT Loss

The NEXT loss that is coupled into a receive lane can be from multiple transmit lanes at the near-end. To ensure the total NEXT loss coupled into a receive lane is limited; a multiple disturber NEXT loss is specified.

2.5 GT/s

The MDNEXT loss between a receive lane and all transmit lanes (e.g., closest in proximity) shall meet the values determined using Equation (6-7).

$$MDNextLoss(f) \geq 31.5 - 17 \times \log\left(\frac{f}{1250}\right) \quad dB \quad 100 \leq f \leq 2500 \tag{6-7}$$

where f is the frequency in MHz.

5.0 GT/s

The MDNEXT loss between a receive lane and all transmit lanes (e.g., closest in proximity) shall meet the values determined using Equation (6-8).

$$MDNextLoss(f) \geq 31.5 - 12.5 \times \log\left(\frac{f}{2500}\right) \quad dB \quad 100 \leq f \leq 7500 \tag{6-8}$$

MDNEXT loss is determined by summing the adjacent individual pair-to-pair differential NEXT loss values using Equation (6-9).

$$MDNextLoss(f) \text{ is defined as } -20 \times \log\left(\sum_{i=1}^{n} 10^{-NextLoss(f)_i / 20}\right) \quad dB \tag{6-9}$$

where f is the frequency in MHz, $NextLoss(f)_i$ is the magnitude in dB of the NEXT loss for frequency f for each measurement i, and n is the number of measurements. If the pair-to-pair NEXT loss measured between 100 MHz and 2500 MHz is greater than 50 dB over the entire frequency range that measurement sweep does not need to be included in the MDNEXT summation.

6.2.2.5. Minimum ELFEXT

Equal level far-end crosstalk (ELFEXT) is specified in order to limit the far-end crosstalk (FEXT) appearing at a Receiver at the far end of a lane (disturbed lane) which is coupled from another lane (disturbing lane) with the noise source (Transmitters) at the near end.

ELFEXT is determined from the differential pair-to-pair FEXT and the insertion loss of the disturbed pair using Equation (6-10).

$$ELFEXT(f) \text{ is defined as } FEXT(f) - InsertionLoss(f) \quad dB \tag{6-10}$$

where f is the frequency in MHz.

2.5 GT/s

The ELFEXT between any transmit lane and any receive lane of a cable assembly shall meet the values determined using Equation (6–11).

$$ELFEXT(f) \geq 25.08 - 20 \times \log\left(\frac{f}{1250}\right) \quad dB \quad 100 \leq f \leq 2500 \tag{6-11}$$

where f is the frequency in MHz.

5.0 GT/s

The ELFEXT between any transmit lane and any receive lane of a cable assembly shall meet the values determined using Equation (6–12).

$$ELFEXT(f) \geq 27.0 - 19.0 \times \log\left(\frac{f}{2500}\right) \quad dB \quad 100 \leq f \leq 7500 \tag{6-12}$$

where f is the frequency in MHz.

6.2.2.6. Minimum Multiple Disturber ELFEXT

Equal level far-end crosstalk (ELFEXT) is specified in order to limit the far-end crosstalk (FEXT) appearing at a Receiver at the far end of a lane (disturbed lane) which is coupled from another lane (disturbing lane) with the noise source (Transmitters) at the near end.

The FEXT loss that is coupled into a receive lane can be from multiple transmit lanes. To ensure the total FEXT loss coupled into a receive lane is limited; a multiple disturber ELFEXT loss is specified.

The MDELFEXT between a receive lane and all transmit lanes (e.g., closest in proximity) shall meet the values determined using Equation (6-13).

$$MDELFEXT(f) \geq 23.08 - 20 \times \log\left(\frac{f}{1250}\right) \quad dB \quad 100 \leq f \leq 2500 \tag{6-13}$$

where f is the frequency in MHz.

MDELFEXT is determined by summing the individual pair-to-pair ELFEXT values using Equation (6-14).

$$MDELFEXT(f) \text{ is defined as } -20\times\log\left(\sum_{i=1}^{n}10^{-ELFEXT(f)_i/20}\right)\quad dB \tag{6-14}$$

where f is the frequency in MHz, $ELFEXT(f)_i$ is the magnitude in dB of the ELFEXT at frequency f for each measurement i, and n is the number of measurements. If the pair-to-pair ELFEXT measured between 100 MHz and 2500 MHz is greater than 40 dB over the entire frequency range that measurement sweep does not need to be included in the MDELFEXT summation.

5.0 GT/s

The MDELFEXT between a receive lane and all transmit lanes (e.g., closest in proximity) shall meet the values determined using Equation (6-15).

$$MDELFEXT\ \ Loss(f) \geq 23.0 - 19.0\times\log\left(\frac{f}{2500}\right)\quad dB\quad 100 \leq f \leq 7500 \tag{6-15}$$

6.2.2.7. Maximum Pair-to-Pair Skew

The difference in propagation delay, or skew, between all cable assembly pair combinations, shall not exceed 1.3 ns; refer to Section 3.2.6.

6.2.2.8. Maximum Intra-Pair Skew

2.5 GT/s

The difference in propagation delay, or skew, between conductors of all cable assembly pairs should not exceed 0.2 UI; refer to Section 3.2.8.

5.0 GT/s

There is not an explicit intra-pair skew requirement for 5.0 GT/s.

6.2.2.9. Maximum DC Resistance Single-Ended Sideband

The resistance of any conductor used for single-ended sideband signaling shall not exceed 10 Ω.

6.2.2.10. Differential-to-Common Conversion Loss

The minimum differential-to-common mode signal conversion loss in the cable assembly shall be determined using Equation (6-16). This specification parameter only applies to cable assemblies operating at 5.0 GT/s.

$$DCMC(f) \geq 18dB\quad 100 \leq f \leq 7500 \tag{6-16}$$

6.2.2.11. HiPot Requirement

The minimum HiPot requirement for cable assemblies shall be 240 VDC for 100 ms.

6.3. Shielding

All cable assemblies shall provide 360 degree shielding from end to end. EMI gaskets may be required at the mating interface to reduce EMI emissions to an acceptable level.

6.4. Active Cables

All cable assemblies have pins assigned for optionally bringing power into each end at the plug to allow for the future development of active cable assemblies that provide features such as active equalization or an electrical to optical interface. Definition of such cable assembly options are beyond the scope of this specification nor are Subsystems required to support active assemblies. Refer to Chapter 4 for additional considerations. Systems also do not provide keying to differentiate between those systems that do provide power and those that do not.

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[1] Company affiliation listed is at the time of specification contributions.